Modeling Reliability of Gallium Nitride

High Electron Mobility Transistors

by

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ABSTRACT

This work is focused on modeling the reliability concerns in GaN HEMT technology. The two main reliability concerns in GaN HEMTs are electromechanical coupling and current collapse. A theoretical model was developed to model the piezoelectric polarization charge dependence on the applied gate voltage. As the sheet electron density in the channel increases, the influence of electromechanical coupling reduces as the electric field in the comprising layers reduces.

A Monte Carlo device simulator that implements the theoretical model was developed to model the transport in GaN HEMTs. It is observed that with the coupled formulation, the drain current degradation in the device varies from 2%-18% depending on the gate voltage. Degradation reduces with the increase in the gate voltage due to the increase in the electron gas density in the channel. The output and transfer characteristics match very well with the experimental data.

An electro-thermal device simulator was developed coupling the Monte Caro-Poisson solver with the energy balance solver for acoustic and optical phonons. An output current degradation of around 2-3 % at a drain voltage of 5V due to self-heating was observed. It was also observed that the electrostatics near the gate to drain region of the device changes due to the hot spot created in the device from self heating. This produces an electric field in the direction of accelerating the electrons from the channel to surface states. This will aid to the current collapse phenomenon in the device. Thus, the electric field in the gate to drain region is very critical for reliable performance of the device. Simulations emulating the charging of the surface states were also performed and matched well with experimental data.

Methods to improve the reliability performance of the device were also investigated in this work. A shield electrode biased at source potential was used to reduce the electric field in the gate to drain extension region. The hot spot position was moved away from the critical gate to drain region towards the drain as the shield electrode length and dielectric thickness were being altered.

Dedicated to my parents,

Mr. M. Padmanabhan and Mrs. P. Rohini

my elder sister, Mrs. P.Krishnaveni

and my dear wife, Mrs. Vasudha Guntur.

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Chapter 1

INTRODUCTION

I. GALLIUM NITRIDE TECHNOLOGY

III-V materials have been emerging as a very strong candidate for high power, high frequency and high temperature applications in the recent years [1,2,3]. The major applications of these devices have been in the blue laser technology and also in microwave power technology. Even though the electron effective mass in the GaN technology is three times when compared to GaAs technology (shown in Table 1), a few distinct advantages have made this a more favorable technology. The first attractive property is the large band gap which lends this technology to be used for power devices with very high breakdown voltages. The second strongest feature of the III-V nitrides is the heterostructure technology that it can support – Quantum well, modulation doped heterointerface, and heterojunction structure can all be made in this system.

In the heterostructure technology, two dimensional electron gas densities of the order of $10^{13}cm^{-2}$ (Figure 1) or higher can be achieved in AlGaN/GaN HEMT devices without intentional doping. This is due to the large piezoelectric polarization of the top strained layer in AlGaN/GaN based transistor structures which is almost five times greater than AlGaAs/GaAs structure. In addition to the piezoelectric polarization effect arising due to the strain, the spontaneous polarization effect which is an inherent property of the material are about 10 times larger for AlN and GaN compared to any other material in the III-V and II-VI semiconductor compounds. The fields produced by the spontaneous charge are in the order of 3 MV/cm and piezoelectric charges are around 2 MV/cm.

These high fields are responsible for high sheet charge density at the interface of the group III nitride material system [4].

Property	Si	GaAs	SiC	GaN
Band gap E_g (eV)	1.12	1.42	3.25	3.40
Breakdown field (MV/cm)	0.25	0.4	3.0	4.0
Electron Mobility μ (cm^2/Vs)	1350	6000	800	1300
Maximum velocity v_d (10^7 cm/s)	1.0	2.0	2.0	3.0
Thermal Conductivity κ (W/cmK)	1.5	0.5	4.9	1.3
Dielectric constant ε	11.8	12.8	9.7	9.0

Table 1: Comparison of semiconductor material properties at 300K.

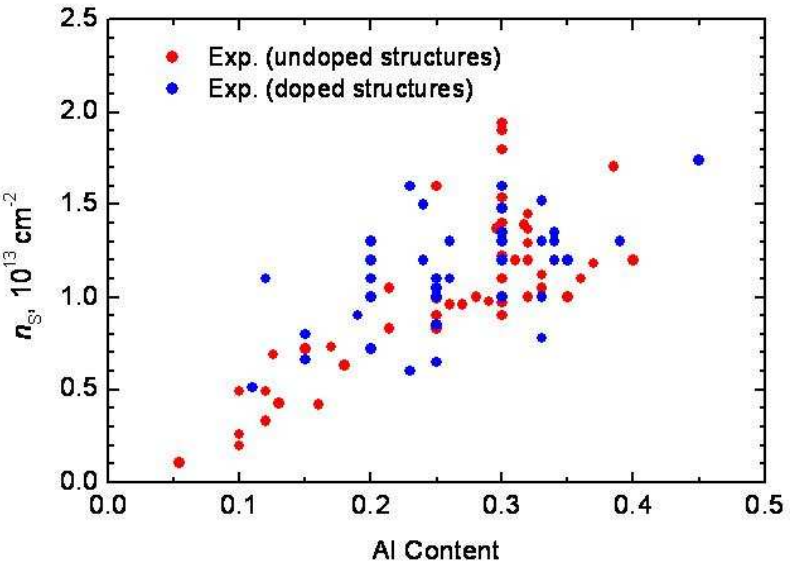

Figure 1: 2DEG sheet concentration in AlGaN/GaN heterostructures vs. Al content x.

II. GALLIUM NITRIDE PROCESSING

The major hurdle in the development curve of the GaN technology is the growth of these materials without defects in comparison to the fact that it is easier to grow silicon and gallium arsenide materials. During earlier years, the direct growth of GaN materials on sapphire and SiC substrates lead to large amount of threading dislocations arising from the substrate interface to the newly deposited thin film. This was mainly due to the high lattice mismatch between the layers [5].

In the late 1980's, Amano *et al.* developed a new methodology to grow high quality GaN film. This was done using a two step process, by using an AlN buffer layer between GaN and the substrate to reduce lattice mismatch (see Figure 2) [6].

To further improve the quality of these GaN films, lateral epitaxial growth technique was employed to heteroepitaxially grow, defect free GaN films. In this method, materials like silicon nitride are deposited on top of GaN substrate. Small windows are etched through to the underlying GaN film and GaN epi is grown through these windows defect free [7].

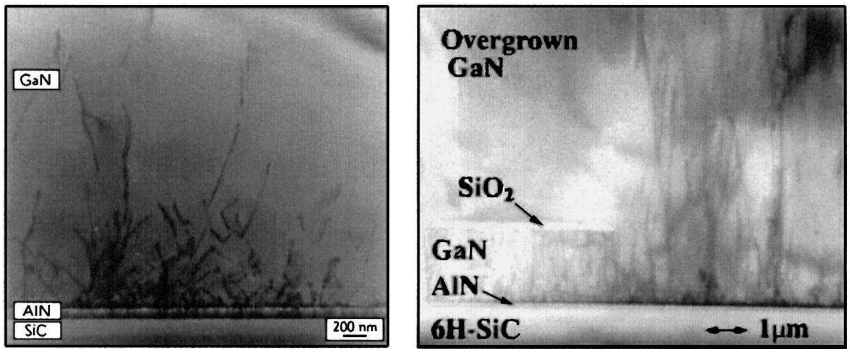

Figure 2: TEM cross-section of MOCVD grown GaN on SiC substrate using AlN buffer layer (left) and LEO grown GaN (right).

III. III-NITRIDE MATERIAL SYSTEM SIMULATIONS: BINARIES & TERNARIES

The electron transport in III-Nitride material systems has been investigated using Monte Carlo simulations since the mid 1970's. One of the earliest works to calculate the velocity field relationship in gallium nitride material was investigated by M.A.Littlejohn, J.R.Hauser and T.H.Wilson in 1975 [8]. The work included implementing polar optical scattering, acoustic scattering, piezoelectric scattering and Coulomb scattering to determine the velocity field characteristics of gallium nitride and its dependence on impurity concentrations.

Since, gallium nitride is used in high electric field conditions, evaluating the electron transport accurately required the inclusion of intervalley scattering mechanism. The dominance of this mechanism leads to a strongly inverted electron distribution and to a large negative differential conductance [9]. A comprehensive study of electron transport in III-Nitride material systems including both binary and ternary materials was investigated in later works. Monte Carlo simulations including all the major scattering mechanisms and band parameters extracted from pseudo potential calculation was implemented. Alloy disorder scattering, being a significant mechanism under very high field conditions in ternary compounds was also implemented to determine the velocity field characteristics of the III-Nitride material system accurately [10]. Alloy disorder scattering was also studied in detail in later works owing to its significance in determining the velocity field characteristics of ternary compounds. Enrico Bellotti. *et al.* developed a Full band Monte Carlo simulation and used a fundamental approach towards implementing alloy disorder scattering based on detailed information from the electronic structure and atomic screened potentials [11].

High thermal stability, extreme hardness and stronger piezoelectric properties than other III-Nitride materials have driven a lot of research towards aluminum nitride material system. Lot of simulation work was done to determine the velocity field characteristics of aluminum nitride material. These works included all the major scattering mechanisms: polar optical phonon scattering, ionized impurity scattering, piezoelectric scattering and intervalley scattering. The piezoelectric scattering mechanism in aluminum nitride was found to play a significant role in determining its velocity field characteristics [12]. It was also observed that aluminum nitride exhibited a much smaller negative differential mobility effect than gallium nitride and the velocity-field characteristics showed a broader peak [13].

IV. III-NITRIDE DEVICE SIMULATIONS

Devices made of III-Nitride materials have also been simulated in the past. Ashwin Ashok from Arizona State University was one of the first to explicitly implement electron -electron interactions with non-parabolic band schemes in GaN diode and investigate its significance under high carrier density conditions [14].

HEMT (High electron mobility transistors) are one of the leading contenders for microwave power applications as mentioned earlier. Various device simulations have been investigated during recent years to understand it's working. One of the significant works was by Yamakawa *et al.* from Arizona State University, where high field transport in GaN HFET was simulated using the cellular based Monte Carlo approach. The work also included quantum mechanical effects. The DC and high frequency characteristics were in good match with experimental data [15].

Detailed HEMT device simulations were also investigated by Ashwin Ashok *et al.* from Arizona State University. The theoretical and simulation aspects of his work are a part of the basic foundation for this research. The various aspects of Ashwin's work, the developments and new formulations in this research work will be explained in detail in the future chapters.

Chapter 2

MODELING OF GaN/AlGaN/AlN/GaN HEMTs

I. ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS

AlGaN/GaN HEMT technology has many advantages, large bandgap, high peak electron velocity, large channel density as explained in the previous chapter. These properties make it highly suitable for high power microwave applications. Nevertheless, this technology also has reliability issues associated with its performance: drain current collapse, formation of cracks at high electric fields etc. One of the main motivations of this work is to investigate these reliability concerns, understanding the physics behind these degradation mechanisms and evaluating various solutions to minimize their impact on the device performance.

In the present study, a GaN/AlGaN/AlN/GaN device is being simulated. Inserting a very thin AlN interfacial layer between the AlGaN and GaN layers helps to increase the sheet charge density and improves mobility of the carriers in the channel. This owes to the reduction of alloy disorder scattering in AlGaN/AlN/GaN HEMT's when compared to AlGaN/GaN HEMT's. Since, the barrier height (conduction band difference) of AlN/GaN layer is larger than AlGaN/GaN layer, the probability of the channel electrons entering the AlGaN layer reduces significantly. This helps in reducing the impact of alloy disorder scattering on the electron mobility, arising from the defects in the AlGaN layer [16,17,18,19].

The increase in conduction band difference also helps to negate the drain current collapse that arises due to traps in barrier and surface states [20]. The other advantage of AlN interfacial layer is to grow a crack free AlGaN layers on GaN template. A high

temperature AlN layer relaxes the stress of between AlGaN and GaN layers thus leading to reduction in defects [21].

II. NUMERICAL MODELING

A. Device Structure

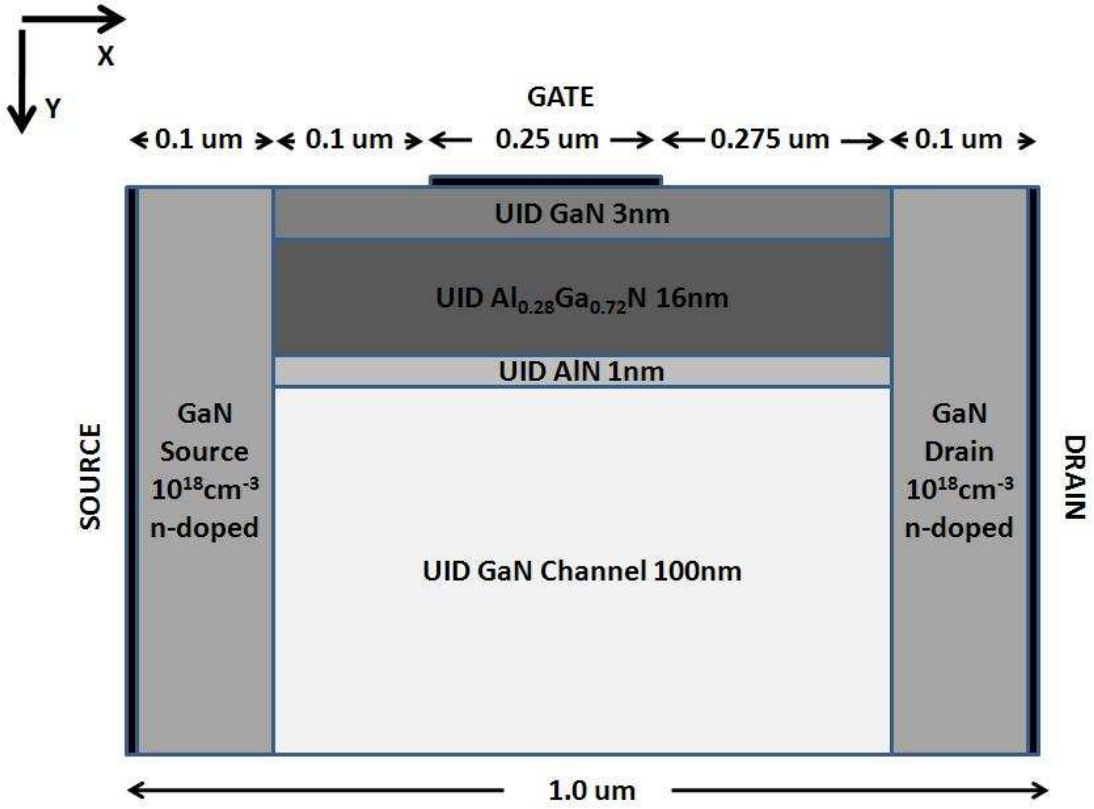

Figure 3: Simulated 2D GaN/AlGaN/AlN/GaN HEMT Structure.

Figure 3 shows the simulated GaN/AlGaN/AlN/GaN HEMT structure. It consists of a 1nm AlN layer grown on 100nm of GaN layer, a 16nm AlGaN layer on the top of AlN layer and a 3nm GaN cap layer. All the layers are unintentionally doped with a doping of 10^{16} cm^{-3}. The source and drain are ohmic contacts and are doped to 10^{18} cm^{-3}. The potential distribution and carrier density in the device structure is simulated by self

consistently solving the two dimensional Poisson equation (potential kernel) with the Monte Carlo routine (transport kernel).

B. 2D Poisson Equation

The potential distribution in any device is calculated by solving the Poisson equation of the form:

$$\nabla.(\varepsilon.\nabla\phi) = q(n - p + N_a - N_d) \tag{2.3}$$

ε is dielectric constant. Na is ionized acceptor concentration.

Φ is electrostatic potential. Nd is ionized donor concentration.

q is elementary charge.

n is electron concentration.

p is hole concentration.

This equation is discretized using the central difference scheme on a 5 point discretization stencil into:

$$\frac{(\varepsilon_{i+1,j} + \varepsilon_{i.j})}{x_i(x_i + x_{i-1})}\phi_{i+1,j} - \left[\frac{(\varepsilon_{i+1,j} + \varepsilon_{i.j})}{x_i(x_i + x_{i-1})} + \frac{(\varepsilon_{i-1,j} + \varepsilon_{i.j})}{x_{i-1}(x_i + x_{i-1})} + \frac{(\varepsilon_{i,j+1} + \varepsilon_{i.j})}{y_j(y_j + y_{j-1})} + \frac{(\varepsilon_{i,j} + \varepsilon_{i.j-1})}{y_{j-1}(y_j + y_{j-1})}\right]\phi_{i,j} + \frac{(\varepsilon_{i-1,j} + \varepsilon_{i.j})}{x_{i-1}(x_i + x_{i-1})}\phi_{i-1,j} + \frac{(\varepsilon_{i,j+1} + \varepsilon_{i.j})}{y_j(y_j + y_{j-1})}\phi_{i,j+1} + \frac{(\varepsilon_{i,j} + \varepsilon_{i.j-1})}{y_{j-1}(y_j + y_{j-1})}\phi_{i,j-1} = q\left(n_{i,j} - p_{i,j} + Na - Nd\right) \tag{2.2}$$

The finite difference approximation of the Poisson equation can be written in the equation of the form Ax=B, where A represents the coefficient matrix, x represents the potential vector to be solved and B represents the forcing function of the vector. The

Poisson equation is linearized to achieve diagonal dominance and leading to faster convergence of the applied numerical method. Boundary conditions are applied at appropriate interfaces. Ohmic contacts follow Dirchilet boundary condition where the potential is fixed and the device is truncated at interface extending to infinity by using Neuman boundary conditions. The Successive over relaxation (SOR) method is used in the current simulator [22].

C. Ensemble Monte Carlo Transport

The transport kernel basically investigates the carrier behavior in the devices, i.e. the probability of finding a carrier with a given momentum **p,** at a particular time **t**, at a given location **r**. This makes the carrier distribution function in the device a six dimensional equation i.e. *f (k, r, t).* The Boltzmann transport equation is solved to calculate this distribution function. The BTE is given by,

$$\frac{\delta f}{\delta t} + v.\nabla_r f + F.\nabla_p f = s(r,p,t) + \left(\frac{\delta f}{\delta t}\right)coll \qquad (2.3)$$

The various moments of the distribution function gives the various parameters of the device that are required.

zeroth moment of the distribution function - particle density

first moment of the distribution function - current density

second moment of the distribution function - energy density

Solving the Boltzmann transport equation is critical to calculate various parameters of the device. The BTE is solved numerically by using the algorithm shown in flow chart in Figure 4. The flow chart in Figure 4 shows the bulk Monte Carlo transport methodology.

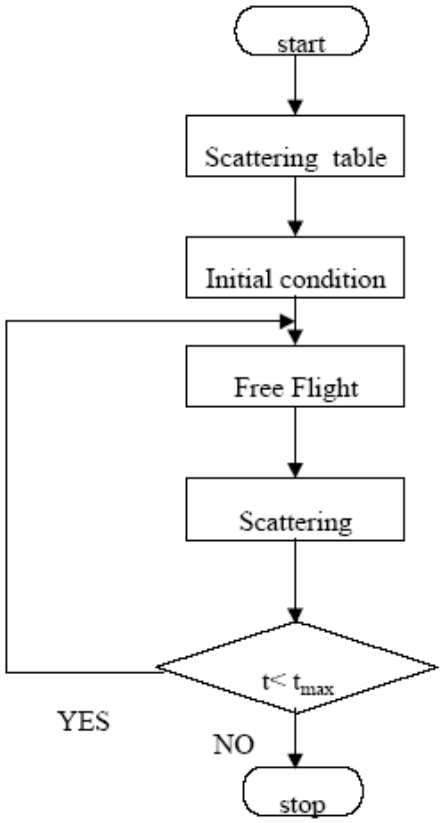

Figure 4: Ensemble Monte Carlo Kernel.

Initially scattering tables are calculated. These scattering mechanisms are normalized to make its selection procedure simpler. Random numbers less than 1 are used to select a particular scattering mechanism. The initialization of the carrier energy for every electron is done using the Maxwell Boltzmann statistics. The momentum of the carrier is also evaluated from the same. The carrier undergoes free flight under the influence of the applied electric field. The momentum of the carrier changes in the direction of the applied electric field as it accelerated and these values in addition to other ensemble quantities are updated at various points of time in the simulation. After finishing the free flight, the carrier undergoes a scattering mechanism which changes the energy and the wave vector the carrier according to the type of scattering mechanism

selected based on its relative importance. The process is continued for a large time scale to obtain steady state condition.

D. Bulk Monte Carlo Transport for AlN

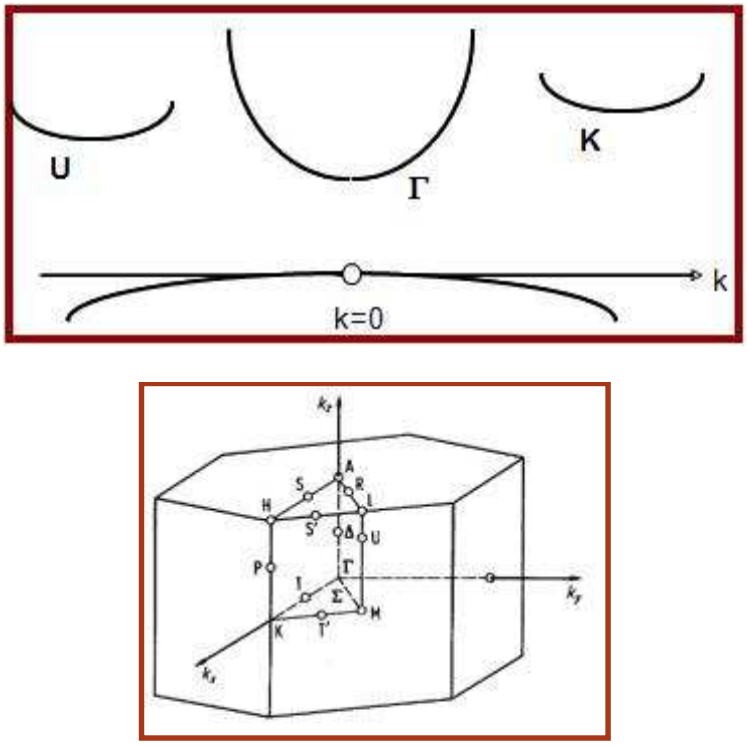

Figure 5: (Top) Band structure of AlN (Bottom) Brillouin zone

Bulk Monte Carlo simulations for AlN were done to obtain its material parameters. The obtained parameters compares very well to prior work (simulation and experimental work). The scattering mechanisms included in these simulations were polar optical phonon scattering, acoustic scattering, Coulomb scattering, intervalley scattering and piezoelectric scattering. A three valley non parabolic band model was used for this simulation (See Figure 5). The material parameters used in the code for AlN are shown in Table 2.

Parameter		Unit	Value
Electron effective mass	Γ	m_e	0.31
	U		0.39
	K		0.54
Non parabolicity constant	Γ	$(eV)^{-1}$	0.32
	U		0.5
	K		0.03
Number of equivalent valleys	Γ		1
	U		6
	K		2
Minimum conduction band energy	Γ	eV	0
	U		0.61
	K		0.67
Static dielectric constant			8.5
High frequency dielectric constant			4.77
Acoustic phonon energy	Γ	eV	10.1
	U		10.1
	K		10.1
Polar optical phonon energy	Γ	meV	99.2
	U		99.2
	K		99.2
Intervalley deformation potential	Equivalent valley transfer	eV/m	$0.5x10^{11}$
	Non equivalent valley transfer	eV/m	$1.0x10^{11}$

Table 2:AlN material properties at 300K.

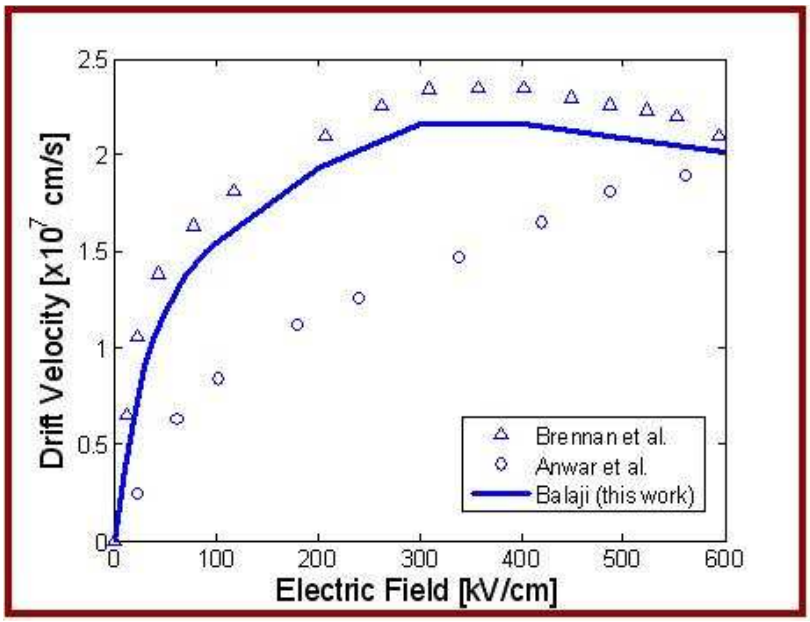

Figure 6: Velocity field characteristics of AlN

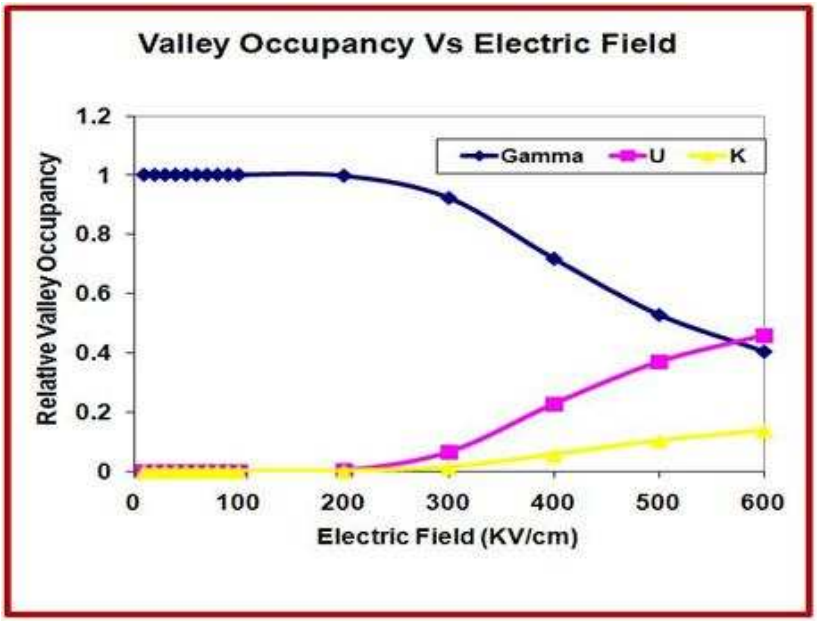

Figure 7: Valley occupancy vs. Electric field characteristics of AlN

The velocity field characteristic in comparison to the prior work and the valley occupancy vs. electric field is shown in Figure 6 and Figure 7 respectively.

E. Concept of Polarization Charge

Crystals made of noncentrosymmetric compounds exhibit two different sequences of atomic layering in two opposite directions parallel to the certain crystallographic axes. Thus, crystallographic polarity can be observed in these crystals. For wurtzite crystal structures, especially for binary A-B compounds the sequence of atomic layer constituting A and B are reversed along [0001] and [0001']. In the case of GaN layers, the general growth direction is normal to the {0001} basal plane where atoms are arranged in bilayers. These consist of two closely spaced hexagonal layers, one formed by cations and the other by anions leading to polar faces. Thus GaN heteroepitaxial layers are either Ga- faced or N- faced. The Ga layer is on the top surface of the {0001} basal plane for the Ga-faced structure. The most important thing to note is that [0001] and [0001'] grown GaN are different and have different physical and chemical properties [23]. The wurtzite Ga- faced and N-faced GaN layers are shown in Figure 8.

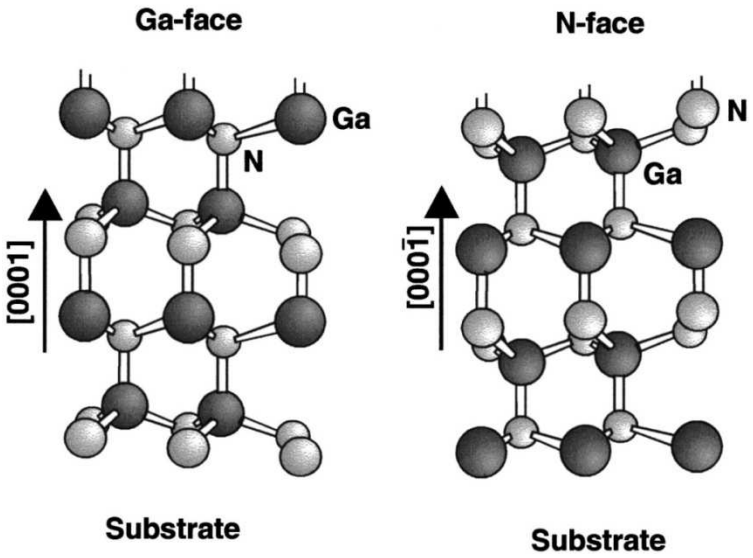

Figure 8: Ga-faced and N-faced wurzite GaN structure.

The total macroscopic polarization charge in GaN, AlGaN or AlN is given by the sum of spontaneous polarization charge P_{SP} of the equilibrium lattice and the piezoelectric or strain induced polarization charge P_{PE}. The spontaneous polarization charge is an inherent property of the material and is very sensitive to the structural parameters. Thus, going from GaN to AlN the spontaneous polarization charge increases due to increasing non ideality in the crystal structure (increasing cation-anion length along the c axes) [23].

The HEMT structures are generally grown along the c axes and the spontaneous polarization along the axes is given by,

$$P_{SP} = P_{SP}z \tag{2.4}$$

The piezoelectric polarization charge is evaluated by,

$$P_{PE} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y) \tag{2.5}$$

where, e_{33} and e_{31} are piezoelectric coefficients.

Here,

$$\epsilon_z = (c - c_0)/c_0 \tag{2.6}$$

where, ϵ_z is the strain along the c axis and

$$\epsilon_x = \epsilon_y = (a - a_0)/a_0 \tag{2.7}$$

The effective polarization charge at any interface is given by,

$$\rho_P = \nabla P \tag{2.8}$$

where, ρ_P is the polarization induced charge density.

$$\sigma = P(\text{Top}) - P(\text{Bottom}) \tag{2.9}$$

$$\sigma = [P_{SP}(\text{Top}) + P_{PE}(\text{Top})] - [P_{SP}(\text{Bottom}) + P_{PE}(\text{Bottom})] \tag{2.10}$$

where, σ is the polarization sheet charge density.

F. Polarization Charge for AlGaN/GaN structures

The piezoelectric polarization charge is negative for tensile strain and is positive for compressive strain. For GaN and AlN, the spontaneous polarization charge is found to be negative. Thus, the direction of spontaneous and piezoelectric charge is parallel in the case of tensile strain and is anti-parallel in the case of compressed strain. If the polarity changes from Ga- faced to N- faced, the sign of the piezoelectric and spontaneous polarization charge also flips. If the net polarization charge at any interface is positive, it will induce free electrons which contribute to the channel 2DEG sheet density. If the net polarization charge at any interface is negative, it induces holes at the interface. The properties of the $Al_xGa_{1-x}N$ barrier layer is given by the linear interpolation of GaN and AlN properties [23],

Lattice constant:

$$a(x) = (-0.077x + 3.189)10^{-10}\text{m} \tag{2.11}$$

Elastic constants:

$$c_{13}(x) = (5x + 103)\ \text{GPa} \tag{2.12}$$

$$c_{33}(x) = (-32x + 405)\text{GPa} \tag{2.13}$$

Piezoelectric constants:

$$e_{31}(x) = (-0.11x - 0.49)\text{C/m}^2 \tag{2.14}$$

$$e_{33}(x) = (0.73x + 0.73)\text{C/m}^2 \tag{2.15}$$

Spontaneous polarization:

$$P_{SP}(x) = (-0.052x - 0.029)\text{C/m}^2 \tag{2.16}$$

The GaN substrate is thick and therefore is not strained. Thus, its piezoelectric component of polarization charge is taken as 0 C/m^2. Therefore, the effective polarization charge at the AlGaN/GaN interface is given by,

$$|\sigma(x)| = |P_{PE}(Al_xGa_{1-x}N) + P_{SP}(Al_xGa_{1-x}N) - P_{SP}(GaN)| \quad (2.17)$$

$$\text{Since, } \sigma = P(\text{Top}) - P(\text{Bottom}) \quad (2.18)$$

The polarization charge at the interface is positive in this case and thus will induce free electrons in the interface forming the channel.

The polarization charge is included in the code as a part of the forcing function in the Poisson equation.

$$\nabla(\varepsilon.\nabla\emptyset) = \rho + \sigma_{\text{polarization}} \quad (2.19)$$

This net polarization charge density is independent of the applied bias and the approach is called the uncoupled formulation.

To fully implement electromechanical coupling into the simulator, the dependence of polarization charge on the applied bias of the device was included. This is called the coupled formulation. This formulation is based on linear piezoelectric constitutive equations of stress and electric displacement given by,

$$\sigma_{ij} = C_{ijkl}\varepsilon_{kl} - e_{kij}E_k \quad (2.20)$$

$$D_i = e_{ijk}\varepsilon_{jk} - k_{ij}E_j + P_i^S \quad (2.21)$$

where, σ_{ij} is the stress tensor,

C_{ijkl} is the fourth rank elastic stiffness tensor,

ε_{kl} is the strain tensor,

e_{kij} is the third ranked piezoelectric coefficient tensor,

k_{ij} is the second rank permittivity tensor,

D_i is the electric displacement,

E_k is the electric field and

P_i^S is the spontaneous polarization.

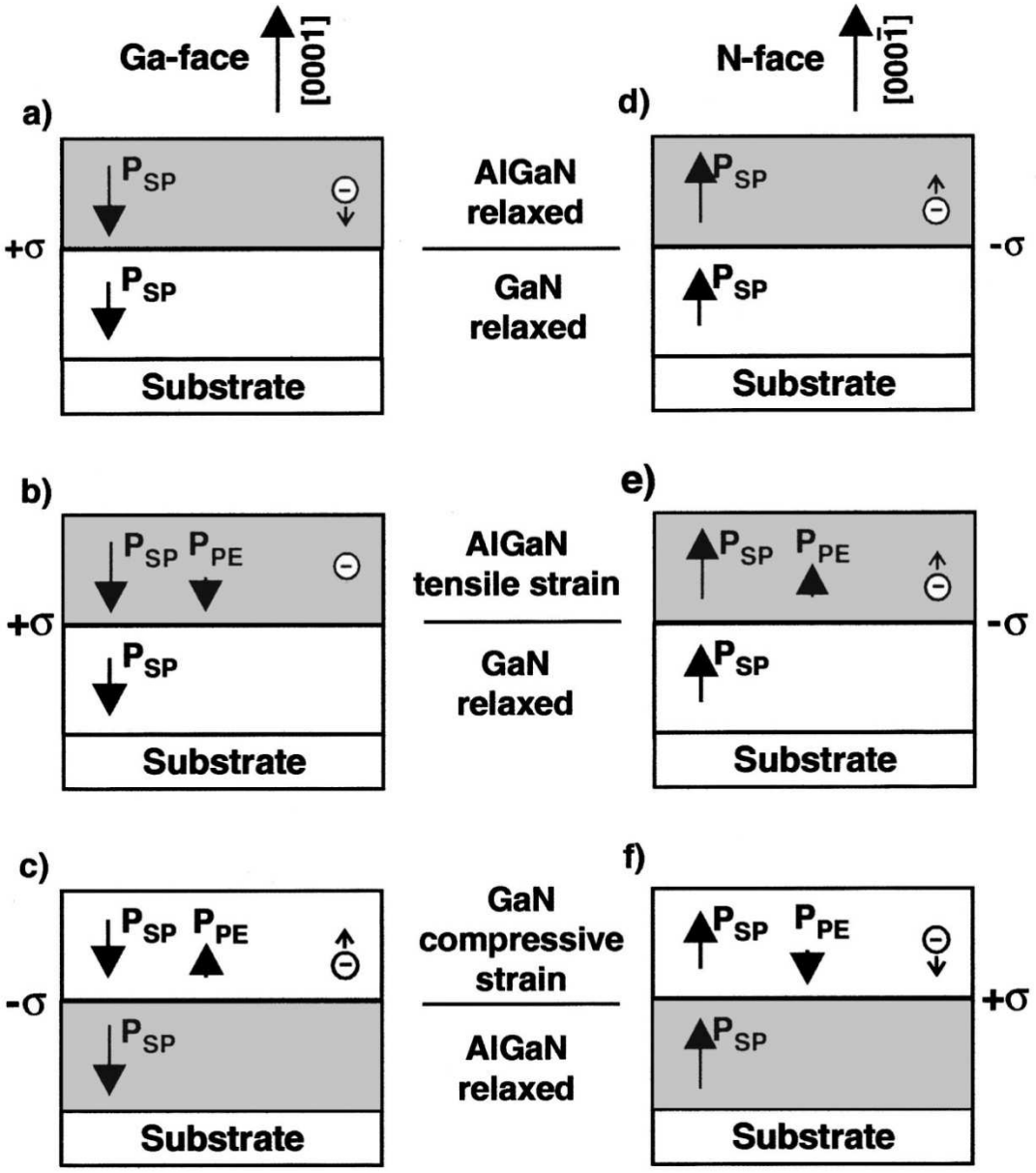

Figure 9: Spontaneous and Piezoelectric polarization charge in Ga-faced and N-faced AlGaN/GaN HEMT.

Considering the AlGaN/GaN structure shown in Figure 9, the GaN layer is assumed to be relaxed as it is thick. The biaxial strain in the thin AlGaN layer satisfies,

$$\epsilon_x = \epsilon_y = (a - a_0)/a_0 \tag{2.22}$$

The absence of stress along the growth direction helps us to represent the strain in the z direction as,

$$\varepsilon_z = -2\frac{c_{13}}{c_{33}}\varepsilon_x + \frac{e_{33}}{c_{33}}E_z^{AlGaN} \tag{2.23}$$

where, E_z^{AlGaN} is the electric field in the AlGaN layer.

The areal charge concentration due to the piezoelectric polarization in AlGaN layer is expressed as,

$$P_{PE}^{AlGaN} = 2\varepsilon_x\left(e_{31} - \frac{c_{13}}{c_{33}}e_{33}\right) + E_z^{AlGaN}\frac{e_{33}^2}{c_{33}} \tag{2.24}$$

In the absence of applied bias or in the uncoupled formulation the second term present in the above equation is equated to 0. The electric field in the AlGaN layer is computed using the perpendicular components of the electric displacement vector at the AlGaN/GaN interface,

$$E_z^{AlGaN} = \frac{1}{k^{AlGaN} + \frac{e_{33}^2}{c_{33}}}\left[\sigma_{2D} + \Delta P^S - 2\varepsilon_x\left(e_{31} - \frac{c_{13}}{c_{33}}e_{33}\right)\right] \tag{2.25}$$

where, k^{AlGaN} is the permittivity of AlGaN layer,

$\Delta P^S = P_{GaN}^S - P_{AlGaN}^S$ is the difference in P_{SP} of GaN and AlGaN layer.

Substituting the electric field expression for AlGaN layer in the piezoelectric polarization equation,

$$P_{PE}^{AlGaN} = 2\varepsilon_x\left(e_{31} - \frac{c_{13}}{c_{33}}e_{33}\right)(1-\alpha) + \alpha(\sigma_{2D} + \Delta P^S) \tag{2.26}$$

$$\alpha = \frac{\left(\frac{e_{33}^2}{c_{33}}\right)}{\left(k^{AlGaN} + \frac{e_{33}^2}{c_{33}}\right)} \tag{2.27}$$

α is the measure of electromechanical coupling.

$\alpha = 0$ corresponds to the uncoupled formulation [24].

G. Polarization Charge for AlGaN/AlN/GaN structures

In the bulk GaN, the 1D Poisson equations may be written far from the GaN/AlN interface,

$$(d^2\Psi/dx^2) = (-qN_D/\varepsilon_3) \tag{2.28}$$

where Ψ represents the electrostatic potential, N_D is the donor concentration and ε_3 is the bulk GaN permittivity.

The solution of the 1D Poisson equation for a bulk GaN slab of thickness 'w', ignoring for the moment the sheet electron density in the triangular potential well and assuming that $\phi_b = \psi(x = w)$ and $\psi(x = 0) = 0$, gives using simple algebra

$$\psi(x) = \frac{qN_D}{\varepsilon_3}\left(wx - \frac{x^2}{2}\right) \tag{2.29}$$

or

$$\phi_b = \varepsilon_3 E_3^2(0)/2qN_D \tag{2.30}$$

where $E_3(0)$ is the electric field at the GaN interface (x=0).

The Fermi potential in the bulk GaN region is given by,

$$\phi_F = \frac{KT}{q}\ln\left(\frac{N_C}{N_D}\right) \tag{2.31}$$

At the AlN/GaN interface, using the Gauss's law one arrives at the following expression for the field in the AlN layer,

$$E_2 = (\varepsilon_3 E_3(0) - q\sigma_2 + qn_{2D})/\varepsilon_2 \tag{2.32}$$

where the various terms appearing in (2.32) are defined in Figure 10. At the AlGaN/AlN interface, the field is given by,

$$E_1 = (\varepsilon_3 E_3(0) - q\sigma_1 + qn_{2D})/\varepsilon_1 \tag{2.33}$$

For the entire structure (Figure 10) one has that,

$$\phi_s + E_1 d_1 + \Delta_1 + E_2 d_2 - \Delta_2 + \phi_b - \phi_F = 0 \qquad (2.34)$$

Substituting all the above equations into (2.34) leads to a quadratic equation for $E_3(0)$.

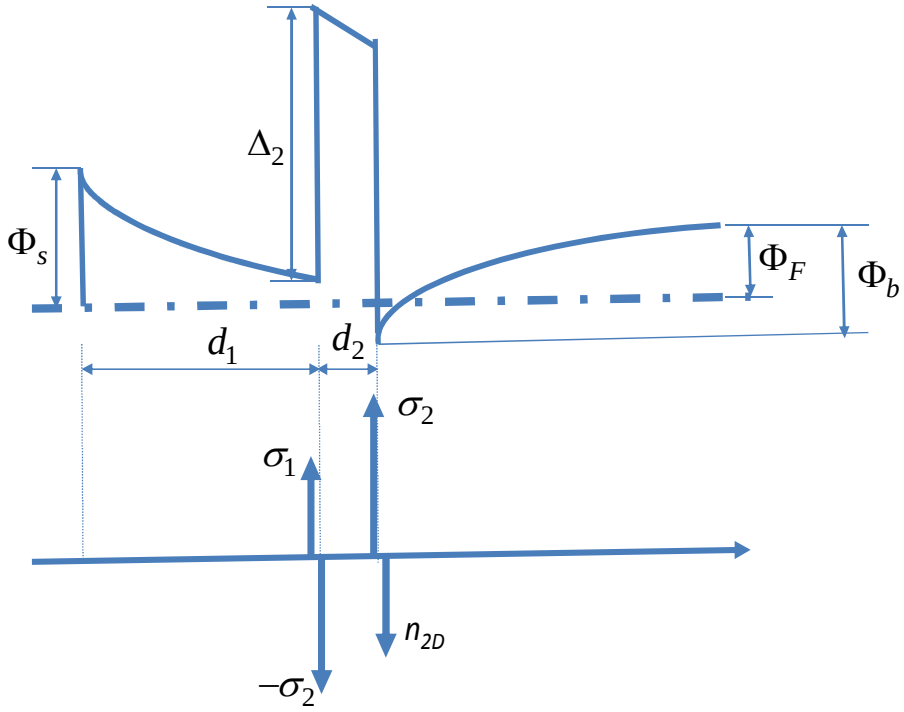

Figure 10: The conduction band profile under zeros gate bias in AlGaN/AlN/GaN structure, defining the various terms appearing in Eqns. (2.28-2.34). The top panel is the conduction band profile and the bottom panel describes the charge densities in the system; d1 is the thickness of the AlGaN layer whose composition is being varied in this study and d2 is the thickness of the AlN layer.

The solution for $E_3(0)$ is used in the expressions for the field in the AlN,E_2 and the field in the AlGaN, E_1.

Having calculated the fields in the various domains allows us to precede with the calculation of the piezoelectric polarization charges at various interfaces using,

$$P_{PE}^{\alpha} = 2\Xi_x^{\alpha}\left(e_{31}^{\alpha} - \frac{c_{31}^{\alpha}}{c_{33}^{\alpha}}e_{33}^{\alpha}\right) + E_z^{\alpha}\frac{e_{33}^{\alpha^2}}{c_{33}^{\alpha}} \quad (2.35)$$

where α represents the layers,

E_z^{α} represents the electric field normal to each layer which is calculated using the theoretical model described above, e_{31}^{α} and e_{33}^{α} are the piezoelectric constants, c_{31}^{α} and $c_{33}^{\alpha}$are the elastic constants and Ξ_x^{α} represents the strain at the surface given by,

$$\frac{a_{bottom\ layer} - a_{top\ layer}}{a_{top\ layer}}$$

where 'a' represents the c-plane lattice constant of the material.

III. SIMULATION RESULTS

A. Theoretical Modeling Results

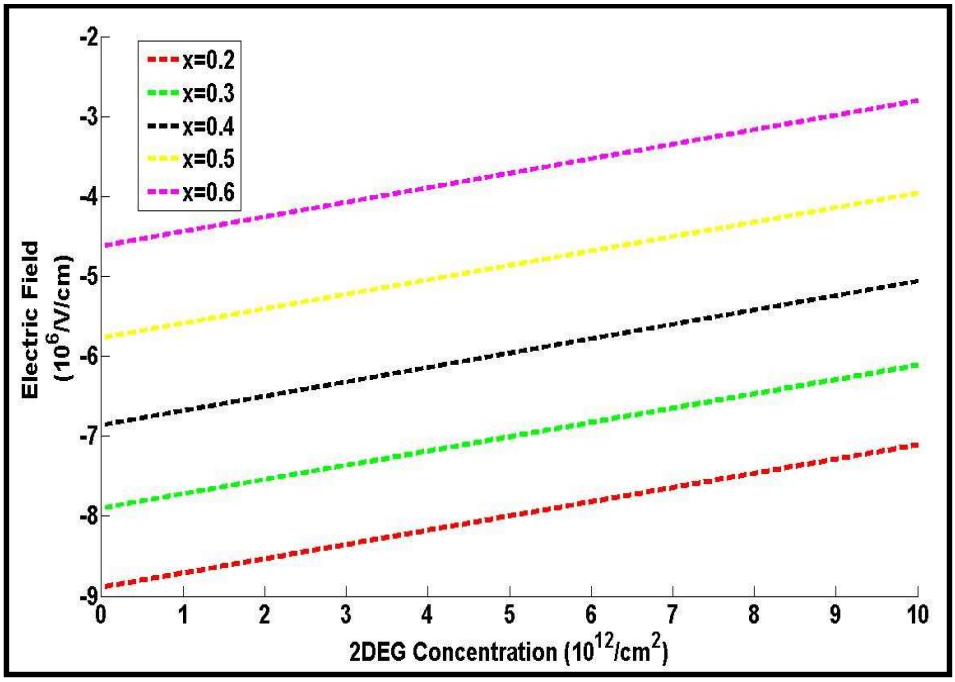

Figure 11: Electric field in the AlGaN layer as a function of 2D sheet electron density, for various mole fractions of Al.

The methodology presented in the previous section is used in the calculation of the sheet electron density and the composition dependence of the electric fields in the AlGaN layer, where current collapse is expected to occur at the drain edge of the gate, as well as in the calculation of the piezoelectric components of the polarization charge density at the AlGaN/AlN and the AlN/GaN interfaces and its modification due to the electromechanical coupling.

With increase in sheet electron density in the channel, the net charge density at that interface decreases and the fields in the AlGaN and AlN layer decrease in absolute value as shown in Figures 11 and 12.

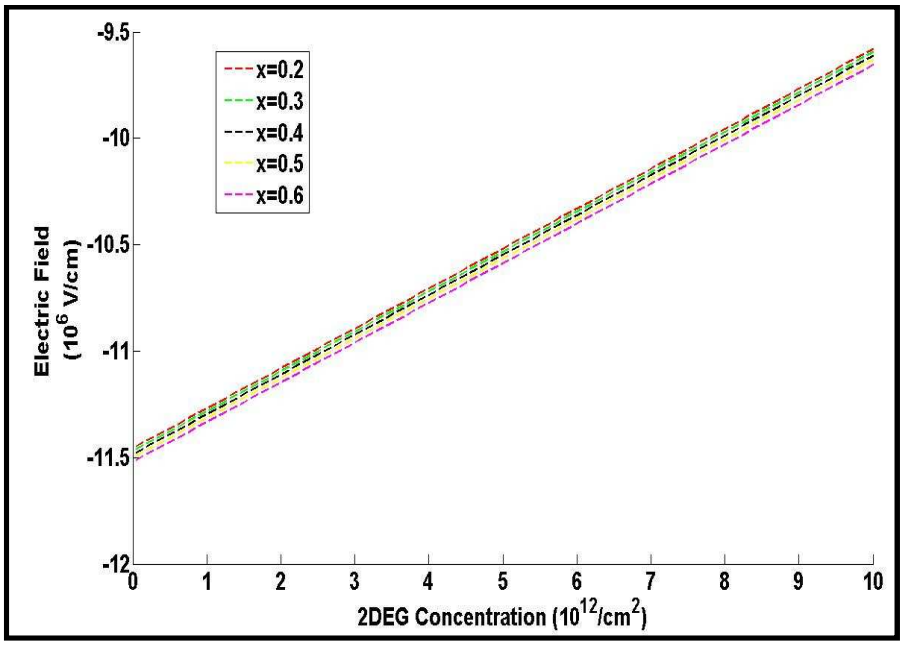

Figure 12: Electric field in the AlN layer as a function of 2D sheet electron density, for various mole fractions of Al.

The reduction in the perpendicular field component, in turn, affects the magnitude of the piezoelectric-component of the polarization charge in the AlGaN and AlN, as shown in Figures 13 and 14. The lower the sheet electron density, the higher the electric

fields in the AlN and AlGaN layers, and the largest is the reduction in the piezoelectric component of the polarization charge density due to electromechanical coupling.

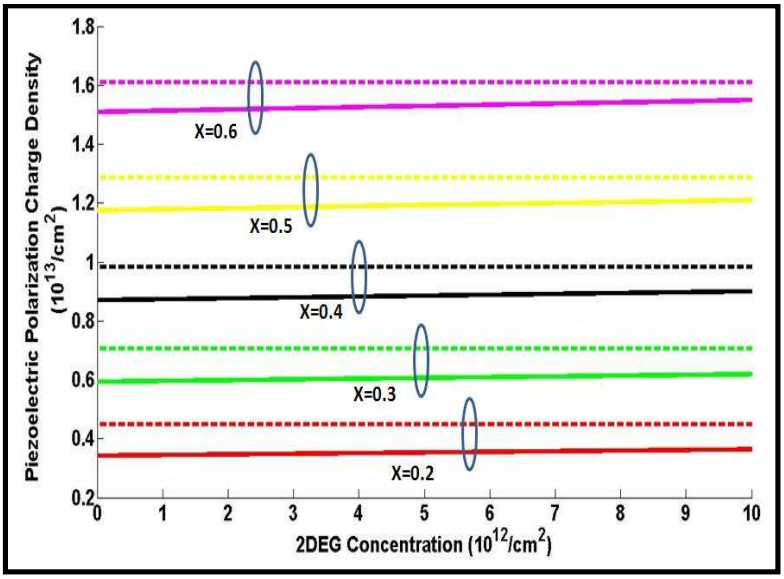

Figure 13: Piezoelectric polarization charge in the AlGaN region as a function of mole fraction and sheet charge density for uncouple (dashed) and coupled (solid) case.

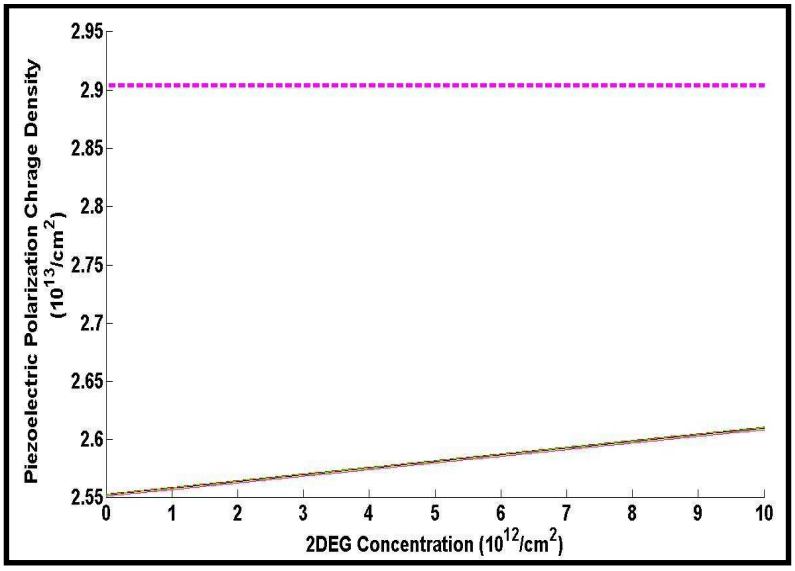

Figure 14: Piezoelectric polarization charge in the AlGaN region as a function of mole fraction and sheet charge density for uncouple (dashed) and coupled (solid) case.

This trend agrees completely with Anwar's work [25]. In fact, for an AlGaN/GaN structure, our model completely reproduces Anwar's results. The work presented here is an extension of Anwar's work and is applicable to arbitrary multilayer structures.

As the sheet electron density increases, since the electric fields decrease, the correction to the piezoelectric polarization charge due to electromechanical coupling is smaller as well. This is clearly illustrated in Figures 13 and 14 for various mole fractions.

B. Implementation of theoretical model in the device structure

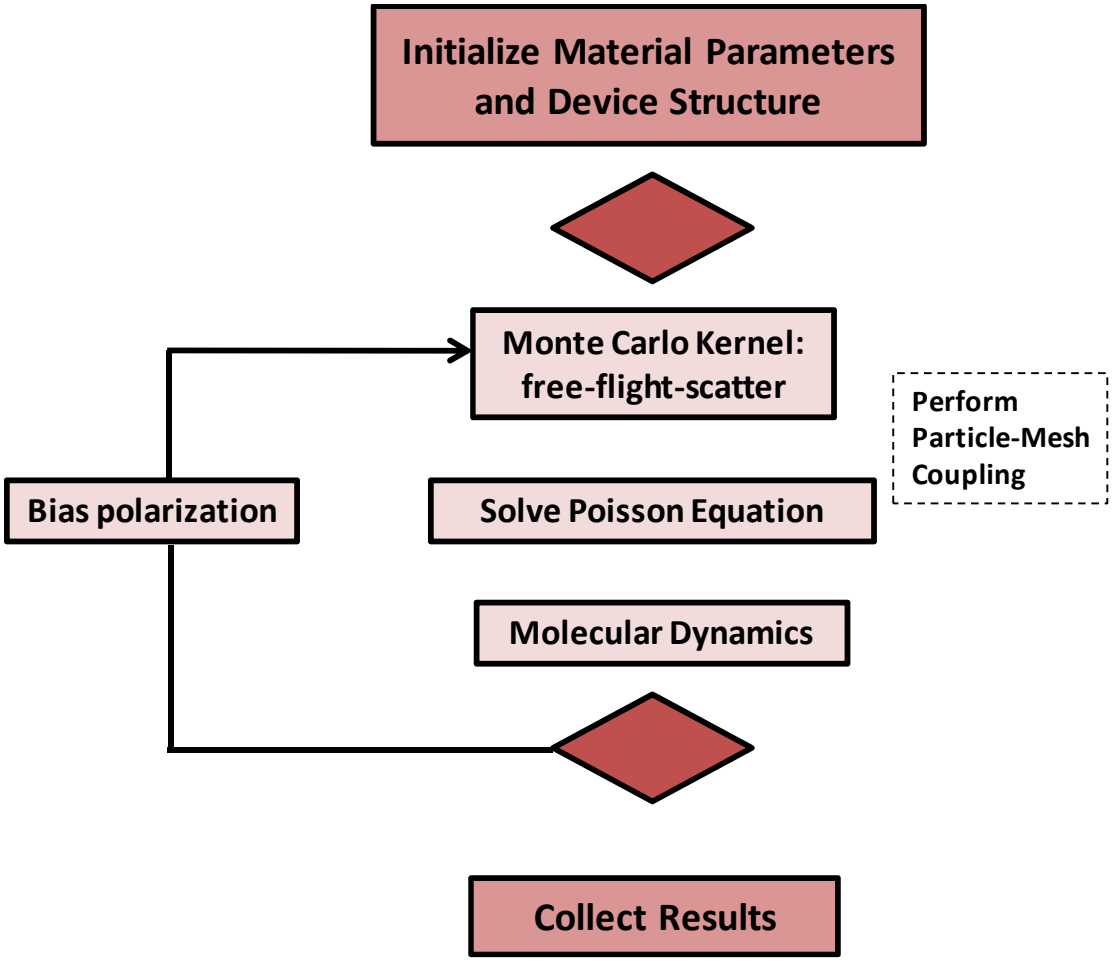

Figure 15: Flow chart of the particular based device simulator

An in-house 2D particle-based device simulator that self consistently solves the Poisson equation coupled with the Monte Carlo transport kernel has been developed to model the gate bias induced strain in GaN heterostructures. The flow-chart of the device simulator, which in a self consistent manner incorporates the electromechanical coupling is shown in Figure 15.

First, the device structure and material parameters is defined and all the simulation variables are initialized. The normalized scattering table for various regions is generated. Initially the Poisson equation is solved for the applied gate bias and the equilibrium solution is obtained. The drain bias is applied and the ensemble Monte Carlo transport routine is solved to obtain the non-equilibrium solution. The electric field is updated using the solution of the Poisson equation and this redistributes the carriers in the device structure during each time step. The carriers undergo a free-flight scatter procedure and the electron density is obtained by counting the number of particles at each mesh, using the Nearest Element Center (NEC) charge assignment scheme. The solution is given to the Poisson solver to generate the updated electric field. The time step is (0.5fs) for the above mentioned process to reach steady state condition. The total simulation time is 10ps for the velocity field characteristics to reach steady state. The average velocities, average energy and output current are calculated.

Transfer and output characteristics were simulated for the device structure shown in Figure 3 for both the uncoupled and coupled polarization models and the effect of gate bias induced strain on the electrical characteristics of the device was evaluated. The simulated output characteristics for varying gate voltage are shown in Figure 16. The Id-Vd characteristics for the uncoupled or constant polarization case matches well with the

experimental characteristics. It is observed from Figure 17 that the coupled formulation leads to degradation in the drain current that varies from 2% to 18%. The degradation in the drain current is the largest near the threshold voltage and reduces for more positive gate voltages. This behavior can be easily explained using the charge argument. Namely for large negative bias, there is almost no inversion charge density in the channel and the vertical fields are high. For zero bias on the gate, the inversion charge is the highest and it balances the net positive spontaneous and polarization charge density, hence the vertical field is the smallest. The same trend is observed in the transfer characteristics as shown in Figure 18.

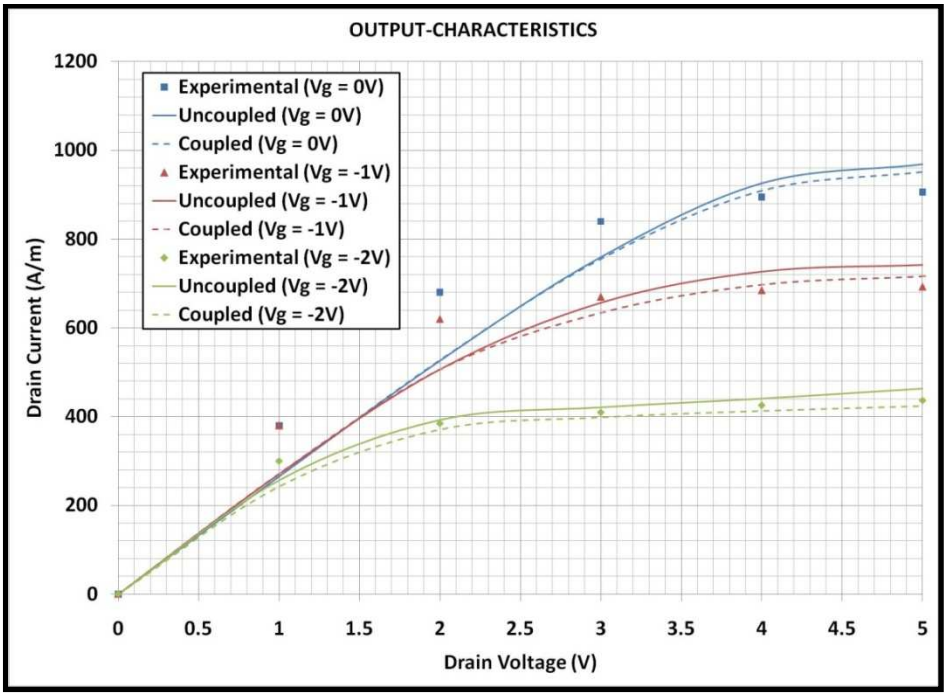

Figure 16: Output characteristics for VG = 0, -1 and -2V

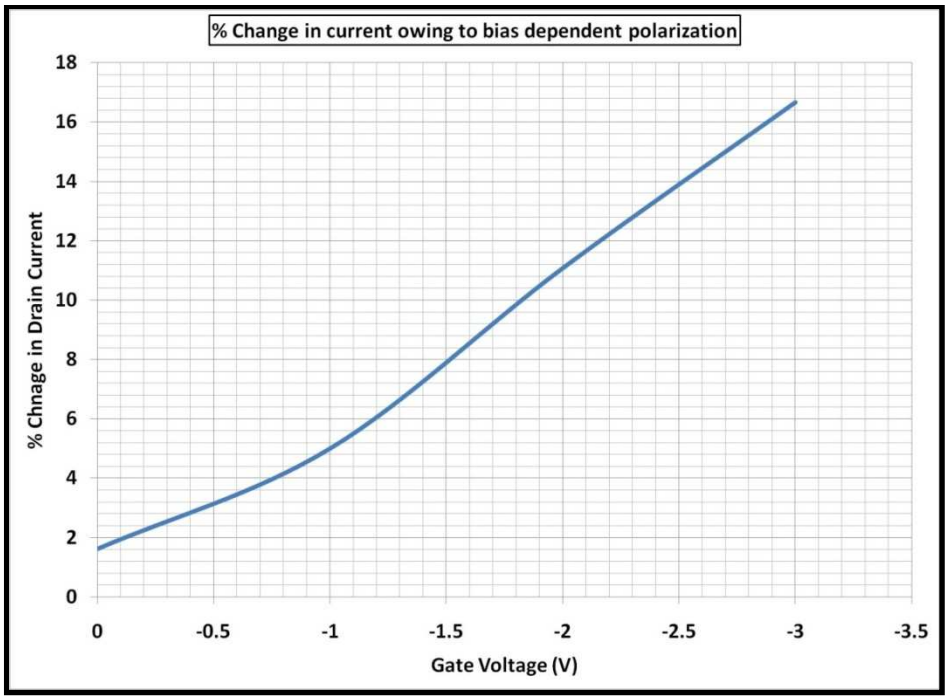

Figure 17: %Change in drain current due to incorporation of electro-mechanical coupling.

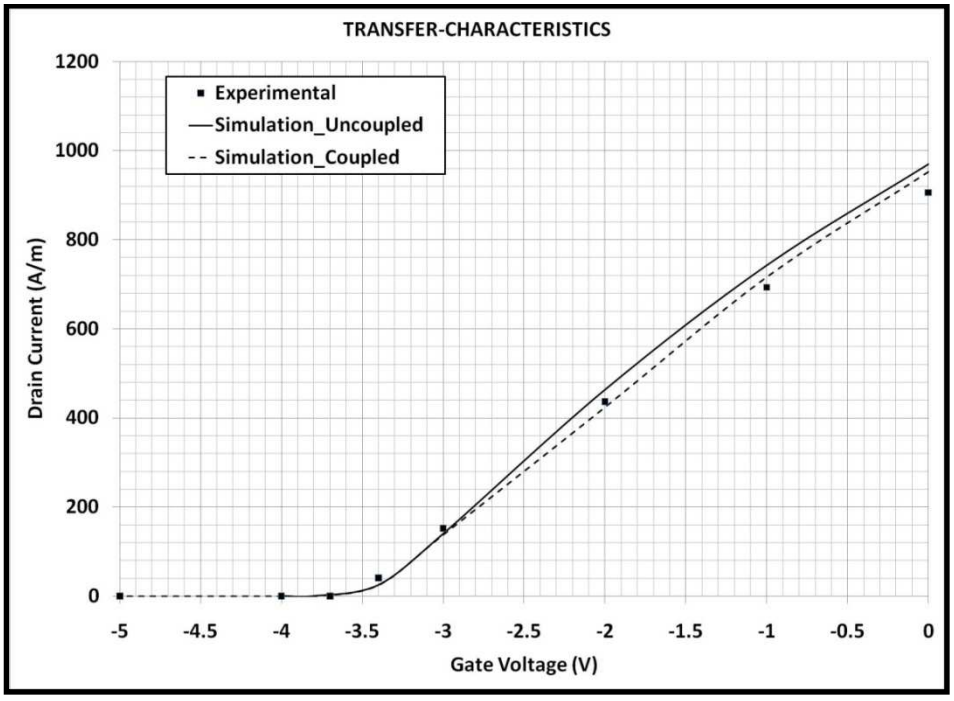

Figure 18: Transfer Characteristics for VD = 5V.

Chapter 3

THERMAL MODELING OF AlGaN/AlN/GaN HEMTs

I. RELIABILITY ISSUES IN GAN HEMTS

GaN HEMTs have been emerging as a strong candidate for high power, high frequency microwave applications owing to their favorable material properties such as larger band gaps, high peak velocity and large saturation velocity. When used in high switching frequency applications and under high power conditions, these devices operate in high thermal regimes. Significant research in the use of GaN material system in such applications have resulted in devices operating with high power densities as high as 32.2 W/mm at around 4GHz for AlGaN/AlN/GaN HEMT with field plates [25]. The combination of high sheet electron densities in the order of $10^{13}cm^{-2}$, higher operating voltages and shrinking device dimensions make the self heating effects in these devices, a significant reliability issue.

Several research studies have indicated that one of the key reliability issues is that the performance of these devices can permanently degrade to varying degrees over short bias stress [26]. The result of self-heating in these devices is the current collapse phenomenon which refers to the degradation of the drain characteristics of the device under DC-stress conditions. It reduces the drain current under saturation conditions, limiting the microwave output power available from the system.

The major reason for this mechanism has been attributed to the trapping/detrapping of electrons in the surface states or trap sites causing RF dispersion effects [27] [28]. The occupied surface states by electrons reduce the 2DEG concentration in the channel by compensating for the spontaneous and piezoelectric

polarization charges at the interface. The correlation of these effects to experiments has been verified in many works but the exact mechanism including trap dynamics, are still to be understood.

II. HEAT TRANSFER IN DEVICES

The transfer of energy from hotter regions of a body to cooler regions by the constituent atoms, molecules or free electrons is called heat. There are basically three modes of heat transfer, conduction, convection and radiation. Conduction is the mode of heat transfer that takes place in solid or fluid materials due to temperature gradient in the system. Heat transfer is related to the measurable scalar quantity called Temperature.

Fourier law is used to explain the heat flow in a homogeneous solid. It is given by,

$$Q(r,t) = -\kappa \nabla T(r,t) \tag{3.1}$$

where Q(r,t) represents the heat flow per unit time, per unit area of the isothermal surface, κ is the thermal conductivity of the material and the temperature gradient is a vector normal to the isothermal surface. The heat flows from a hotter to a cooler region, making the heat flux point in the direction of decreasing temperature. Therefore, a minus sign is included in the equation (3.1) to make it a positive quantity. This equation clearly shows that the thermal conductivity of the system is a very important property for heat flow.

The above formulation holds good for macroscopic systems but fails for micro scale systems due to both classical and quantum size effects [29]. Heat is transported in dielectrics by phonons, which are quantized lattice waves [30]. They can be treated as both particles and waves depending on the characteristics length of the structure in

comparison to the phonon characteristic lengths. The classical size effect is when phonons are treated as particles and the wave effect is when phonons are treated as waves. Figure 19 shows the phonon transport over different characteristics lengths of the structure with the dominant phonon mean free path and wavelength at room temperature.

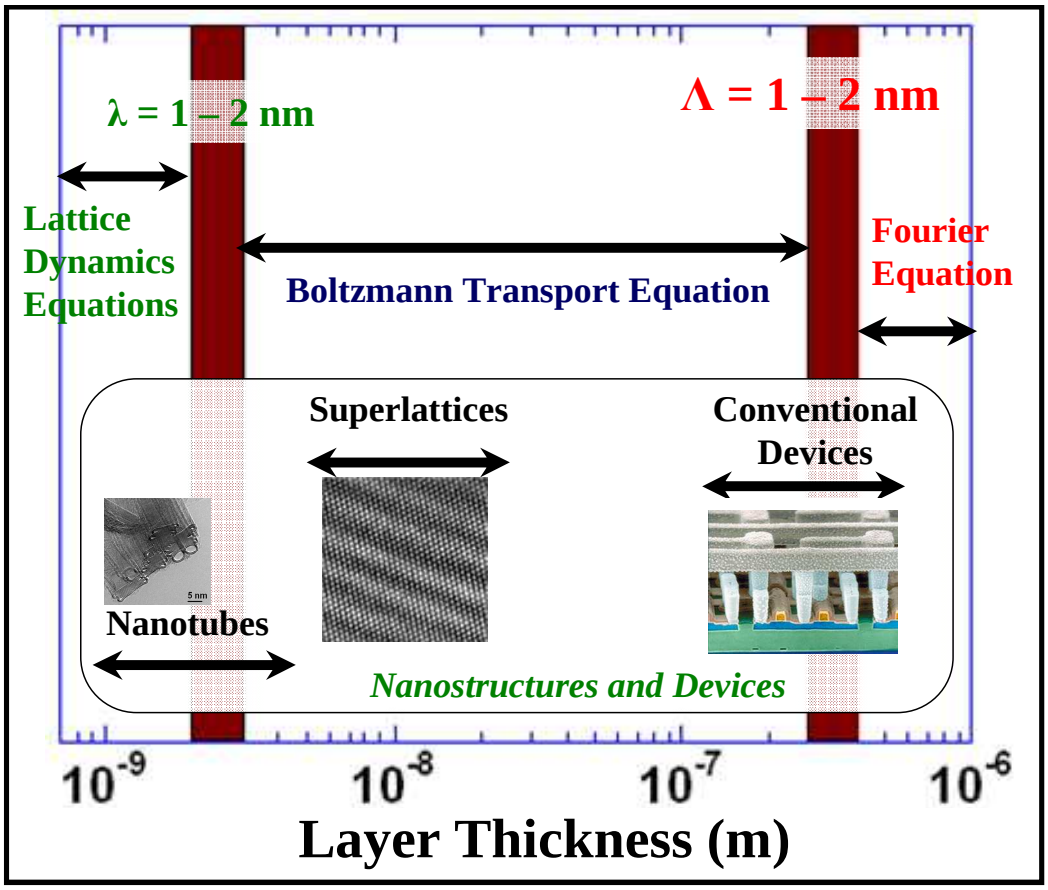

Figure 19: Phonon transport over different characteristic lengths

To model the heat transport in devices, three models are commonly used: (1) Joule Heating, (2) electron-lattice scattering and (3) phonon model. In commercial simulators the inclusion of heat using the Fourier law does not take into consideration the microscopic transfer of heat and the non equilibrium between the acoustic and optical phonon baths.

To study the thermal non equilibrium in submicron MOSFETs, Lai and Majumdar developed a coupled electro thermal model. The highest electron and lattice temperatures occurring at the drain side of the gate electrode has been proved in their study [31]. Raleva *et al*. at ASU, solved the Boltzmann Transport equation (BTE) for electrons using the ensemble Monte Carlo (EMC) method coupled with moment expansion equations for both acoustic and optical phonons [32]. In the present work, the same approach has been followed.

III. ELECTRO-THERMAL SIMULATOR

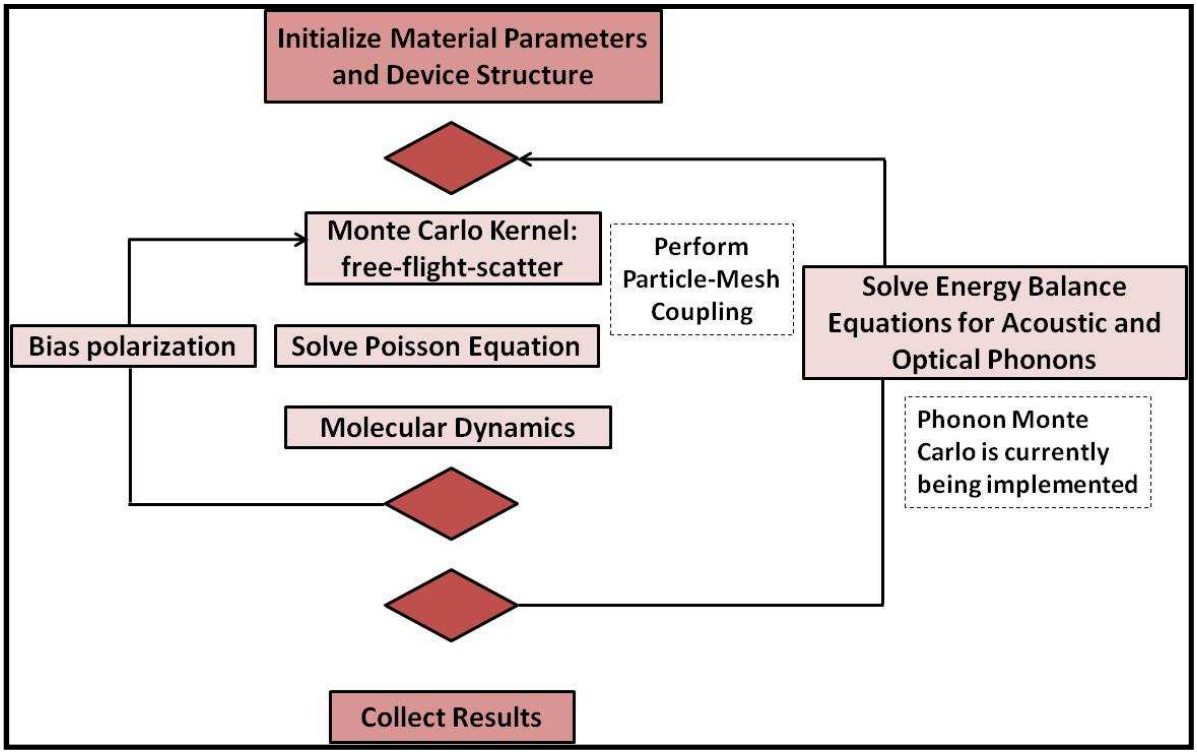

Figure 20: Flow chart of the electro-thermal particle based device simulator.

The need for a separate treatment of the optical and acoustic phonons comes from the very nature of the heat dissipation in the device. As shown in Figure 21, the energy of the electrons gained by the electric field is very quickly transferred to the optical phonons

and some smaller portion to the acoustic phonons. The reason for this is that zone-center optical phonons have much higher energy compared to zone-center acoustic phonons. The energy given to the optical phonon bath does not propagate due to the almost negligible group velocity of the optical phonons. Thus, a hot spot forms in the region where the energy of the electrons is the largest. Over much longer time scale, the optical phonons via anharmonic processes decay into acoustic phonons, and the acoustic phonons eventually transfer the heat away from the hot spot.

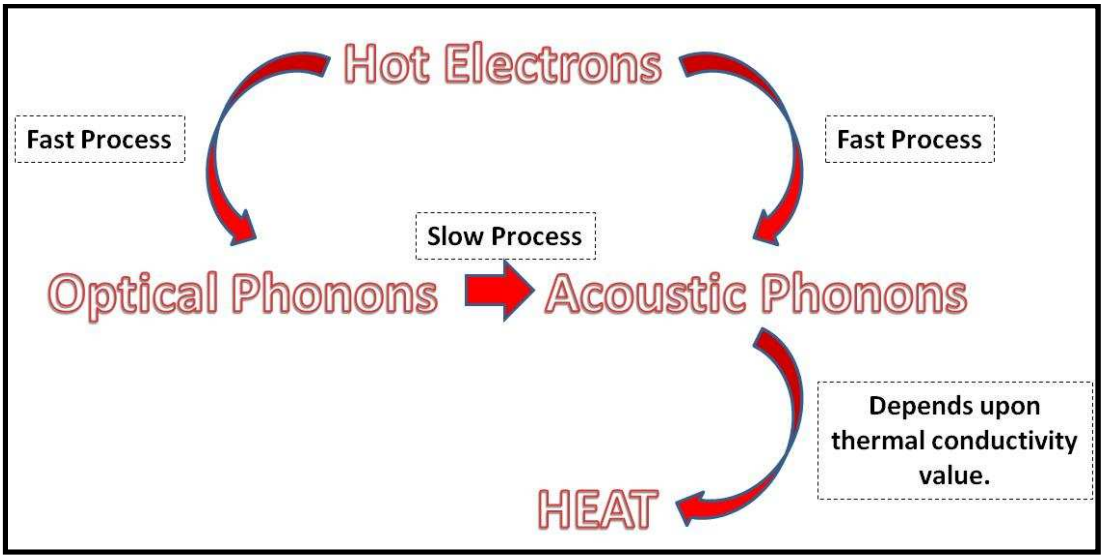

Figure 21: Transport of energy in the electron-phonon system

The BTE for the two kinds of phonons is used to provide the energy balance of the processes illustrated in Figure 3. This means, coupling the electron BTE with the equations for the optical and the acoustic energy transfer (that are derived from the phonon BTE) of the form:

$$C_{LO}\frac{\partial T_{LO}}{\partial t} = \frac{3nk_B}{2}\left(\frac{T_e - T_L}{\tau_{e-LO}}\right) + \frac{nm.v_d^2}{2\tau_{e-LO}} - C_{LO}\left(\frac{T_{LO} - T_A}{\tau_{LO-A}}\right) \quad (3.2a)$$

$$C_A\frac{\partial T_A}{\partial t} = \frac{3nk_B}{2}\left(\frac{T_e - T_L}{\tau_{e-L}}\right) + \nabla.(k_A\nabla T_A) + C_{LO}\left(\frac{T_{LO} - T_A}{\tau_{LO-A}}\right) \quad (3.2b)$$

The first two terms in the right-hand side of (3.2a) represent the energy gain from the electrons, where n is the electron density and v_d is the drift velocity, while the last term is the energy loss to the acoustic phonons. The latter appears as a gain term on the RHS of (3.2b). The first term on the RHS of (3.2b) accounts for the heat diffusion and the last term must be excluded if the electron-acoustic phonon interaction is treated as elastic. In this term, the lattice temperature T_L is estimated as equivalent to T_A.

Note that proper boundary conditions accounting for the heat sink apply for (3.2b).C_{LO} and C_A represent the heat capacity of optical and acoustic phonons respectively, and k_A is the thermal conductivity.

In our simulator, the electron temperature is obtained from the EMC time averages. Not that the existing state of the art in this area is non-self-consistent solver that has been recently developed by Raman et al [33]. This group first solves the hydrodynamic transport model for the electrons to get the electron data and then, as a post processing scheme, solves (3.2a)-(3.2b) to get the proper lattice temperature distribution.

In our research effort the EMC code for the carrier BTE solution [34] [35] has been modified as well. With variable lattice temperature in the hot-spot regions, the concept of temperature dependent scattering tables is introduced. For each combination of acoustic and optical phonon temperature, one energy dependent scattering table is created. These scattering tables involve additional steps in the Monte Carlo phase, because to choose randomly a scattering mechanism for a given electron energy, it is necessary to find the corresponding scattering table. To do that, first, the electron position on the grid needs to be found, in order to know the acoustic and optical phonon

temperatures in that grid point, and then the scattering table with coordinates (T_L,T_{LO}) is selected. Using current state of the art computers, the pre-calculation of these scattering tables does not require much CPU time or memory resources and is done once in the initialization stages of the simulation for a range of temperatures. An interpolation scheme is then adopted afterwards for temperatures for which the appropriate scattering table is not available.

To properly connect the particle-based picture of electron transport with continuous, “fluid like” phonon energy balance equations, a space-time averaging and smoothing of electron density, drift velocity and electron energy are included. At the end of each MC step, the electrons are included. At the end of each MC time step, the electrons are assigned to the nearest grid point. Then, the drift velocities and thermal energies are averaged with the number of electrons at the corresponding grid points. After the MC phase, a time averaging of electron density, drift velocity and thermal energy is done and the electron temperature distribution is calculated. It is assumed that the drift energy is much smaller than the thermal energy. The smoothing of these variables is necessary, because most of the grid points, especially at the interfaces, are rarely populated with electrons. This leads to very low lattice temperatures in those points. The exchange of variables between electron and phonon solvers is shown in Figure 22.

Important fact worth mentioning here is that the present work builds upon the previous work in our research group and adds in a more quantitative manner, the spatial variations of the thermal conductivity. It also has improved methodology for the averaging technique for the electron density; drift velocity and electron energy which in turn leads to faster convergence. With these modifications more accurate description of

the hot spot and the heat transport through the structure is obtained. In what follows, the application of the electro-thermal particle-based device simulator for modeling self-heating effects in GaN HEMTs.

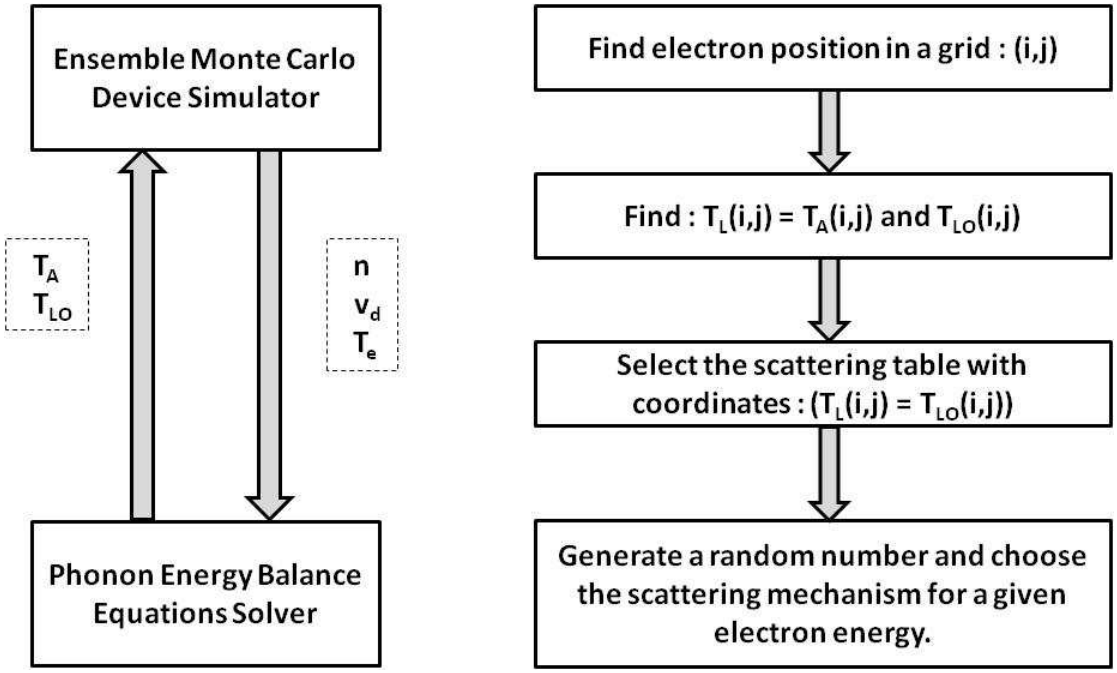

Figure 22: (Left Panel) Exchange of variables between the two kernels (Right Panel) Choice of the proper scattering table.

IV. SIMULATION RESULTS

The structure under investigation is shown in Figure 3. The source and drain are doped to $10^{18}cm^{-3}$. This is relatively low doping that introduces source and drain series resistance for which the final results have to be corrected. Simulations were run with the electro-thermal particle based device simulator described in the previous section. The Monte Carlo device simulation was run for 10ps after which the energy balance equations for the acoustic and optical phonon temperatures were solved. This corresponds to one Gummel loop or one Gummel cycle. Figure 23 and Figure 24 show the convergence of the algorithm based on maximum lattice temperature in the device (assumed the same as acoustic phonon temperature), and on the maximum electron temperature.

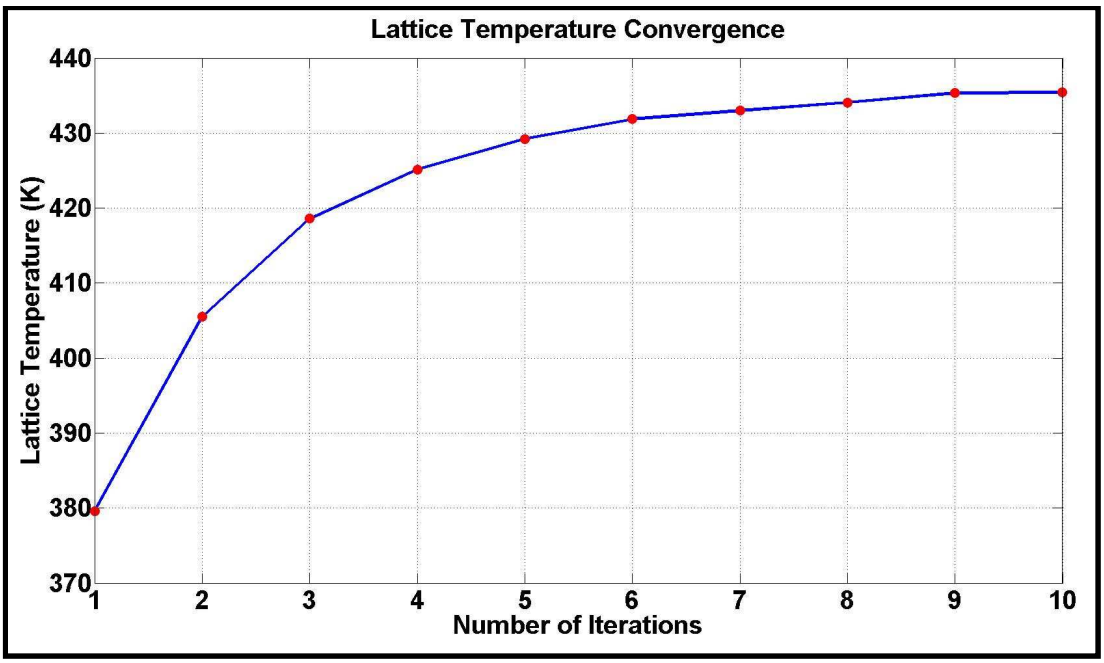

Figure 23: Maximum Lattice Temperature in the device Vs. Gummel cycles

(Phonon relaxation time 0.2ps)

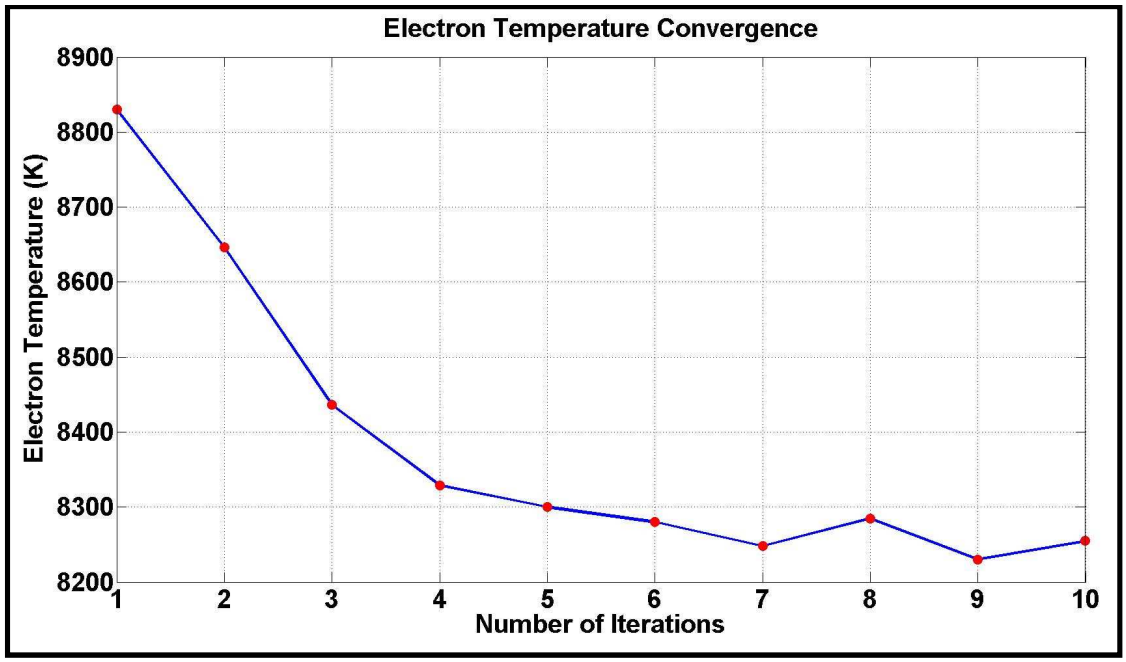

Figure 24: Maximum Electron Temperature in the device Vs. Gummel cycles

(Phonon relaxation time 0.2ps)

The simulations were run for bias conditions of V_{GS} = 0V and V_{DS} = 9V. As can be observed, a minimum of 9 Gummel cycles are needed to reach convergence, which is relatively small. As can be seen, as the lattice temperature increases, there is commensurate decrease of the peak electron velocity, which is related to the reduction of current, as discussed later.

An important parameter related to the reliability of GaN HEMT's is the lattice temperature profile shown in Figure 25. It is evident from the figure that the hot-spot is near the drain end of the channel where the electron temperature is highest (Figure 26), and is shifted slightly towards the drain end on the lattice temperature profile (Figure 25) due to the finite group velocity of the acoustic phonons. More importantly, the hot spot extends both towards the gate and towards the channel. The substrate used in the

simulation is GaN with the back surface being one of the thermal boundary conditions and the gate electrode being the other.

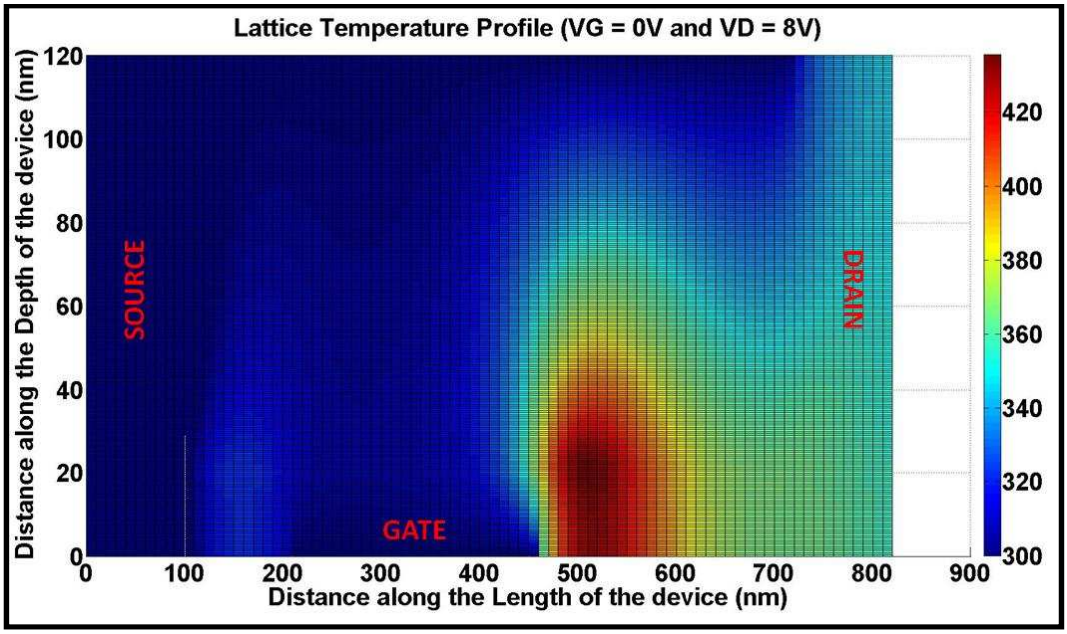

Figure 25: Lattice Temperature Profile

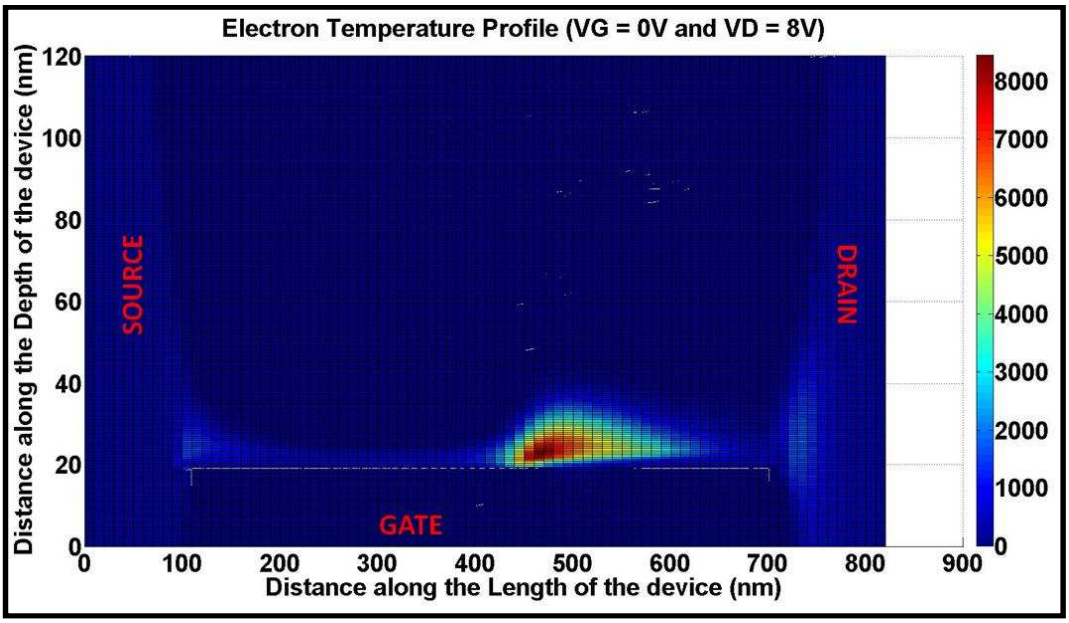

Figure 26: Electron Temperature Profile

An important parameter related to the reliability of GaN HEMT's is the lattice temperature profile shown in Figure 25. It is evident from the figure that the hot-spot is near the drain end of the channel where the electron temperature is highest (Figure 26), and is shifted slightly towards the drain end on the lattice temperature profile (Figure 25) due to the finite group velocity of the acoustic phonons. More importantly, the hot spot extends both towards the gate and towards the channel. The substrate used in the simulation is GaN with the back surface being one of the thermal boundary conditions and the gate electrode being the other.

The peak lattice and electron temperature variation with the electron to optical phonon relaxation time has been plotted in Figure 27. It is observed that with the increase in relaxation time, the peak lattice temperature decreases and the peak electron temperature increases due to the reduction of scattering.

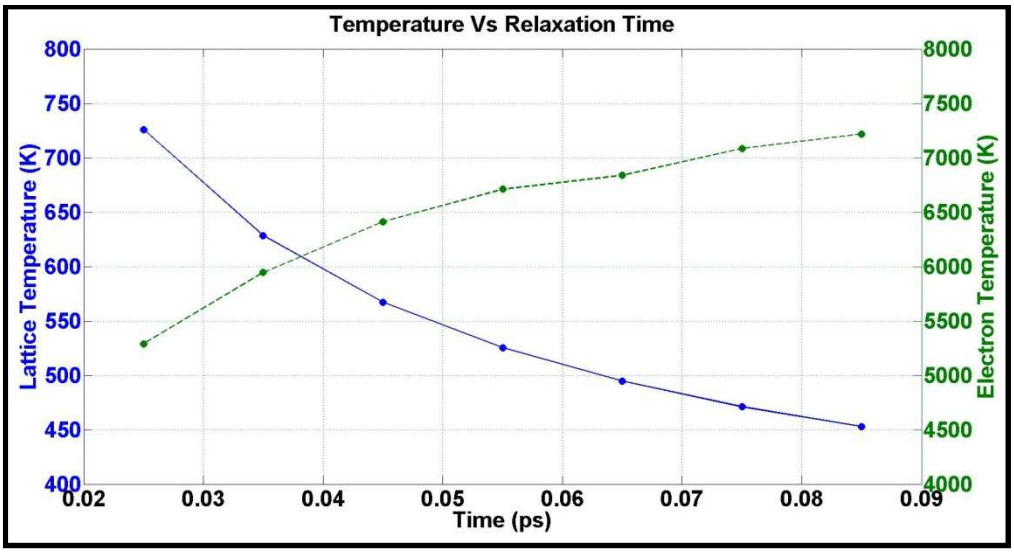

Figure 27: Maximum Lattice and Electron Temperature Vs Phonon relaxation time (VG = 0V and VD = 8V)

The modification of the electrostatics when self-heating effects are accounted for modifies the magnitude of the electric field. This is clearly shown in Figure 28 where the y-component (along the growth direction) of the difference of the electric field for the case when self-heating effects are accounted for and for the case when self-heating effects are not accounted for (isothermal case) has been plotted.

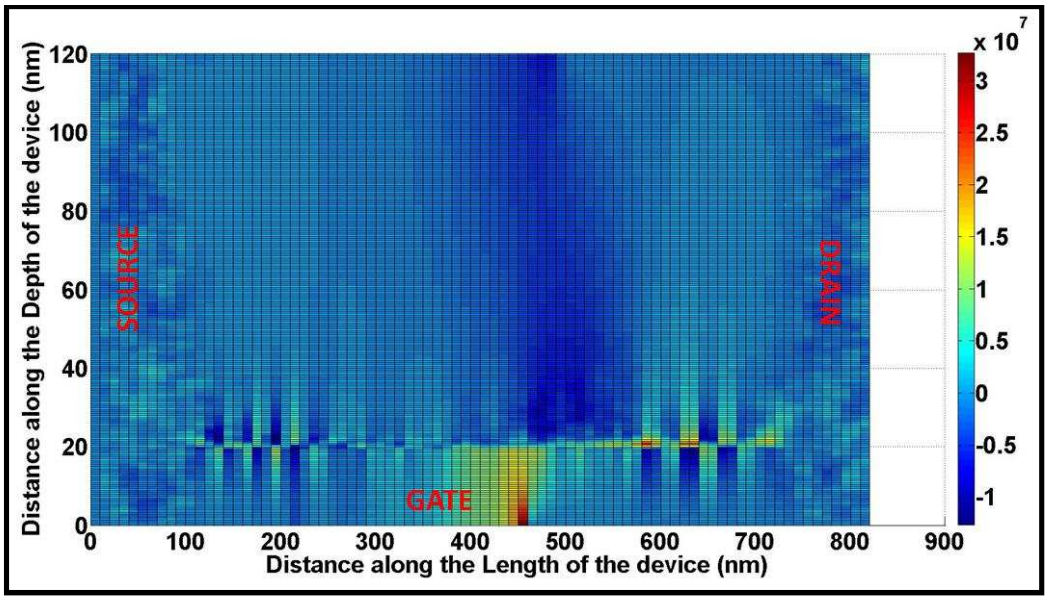

Figure 28: Difference between the vertical component of electric field in the simulation including self heating effects and excluding the same.

Figure 28 shows that the net field difference is positive near the gate-drain extension thus contributing to a larger probability that the channel electrons are being accelerated towards the surface and increasing the occupancy or hot carrier generation of surface states. This compensates the charge in the channel and reduces the magnitude of the on-current current collapse). The drain current for VG = 0V for the isothermal and the non-isothermal case is shown in Figure 29.

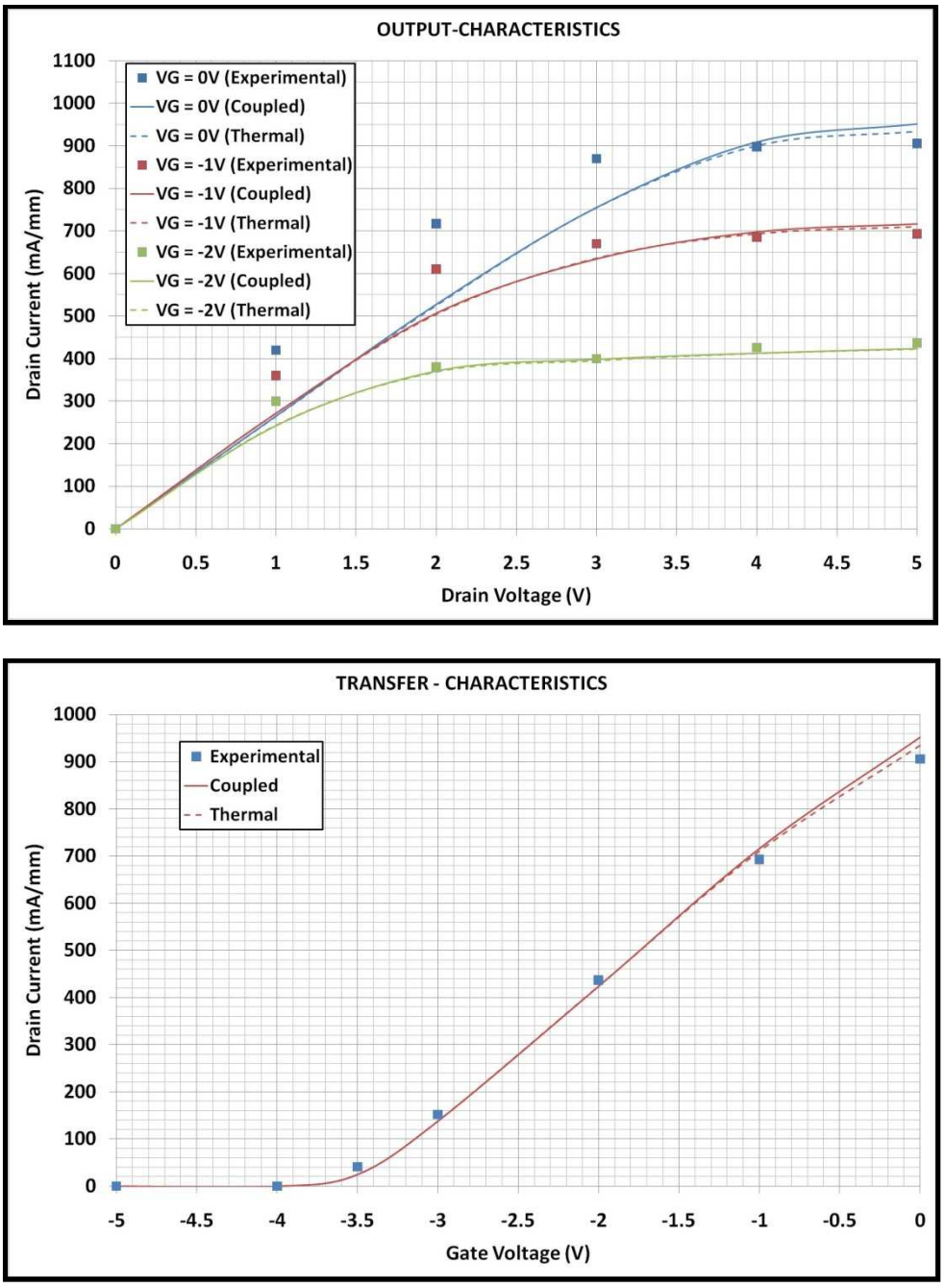

Figure 29: (Top) Output Characteristics for VG = 0V, (Bottom) Transfer Characteristics

Excellent agreement between the non-isothermal case and the experimental data in particular in the saturation region has been obtained. For Vds = 5V, self heating leads to current degradation of around 2-3%. Larger current degradations are expected for

higher drain biases. The temperature increase is localized in the drain end of the channel and not the entire channel and the amount of degradation correlates to this factor.

V. CHARGING OF SURFACE STATES

Current collapse occurs due to the charging of the defects in the material system and also due to the charging of the surface states as explained in the previous section. To emulate the effect of the charging of the surface states on the performance of the device, simulations were performed with negative charges on the surface near the gate to drain region. The output characteristics of the device for various amounts of charge on the surface are shown in Figure 30.

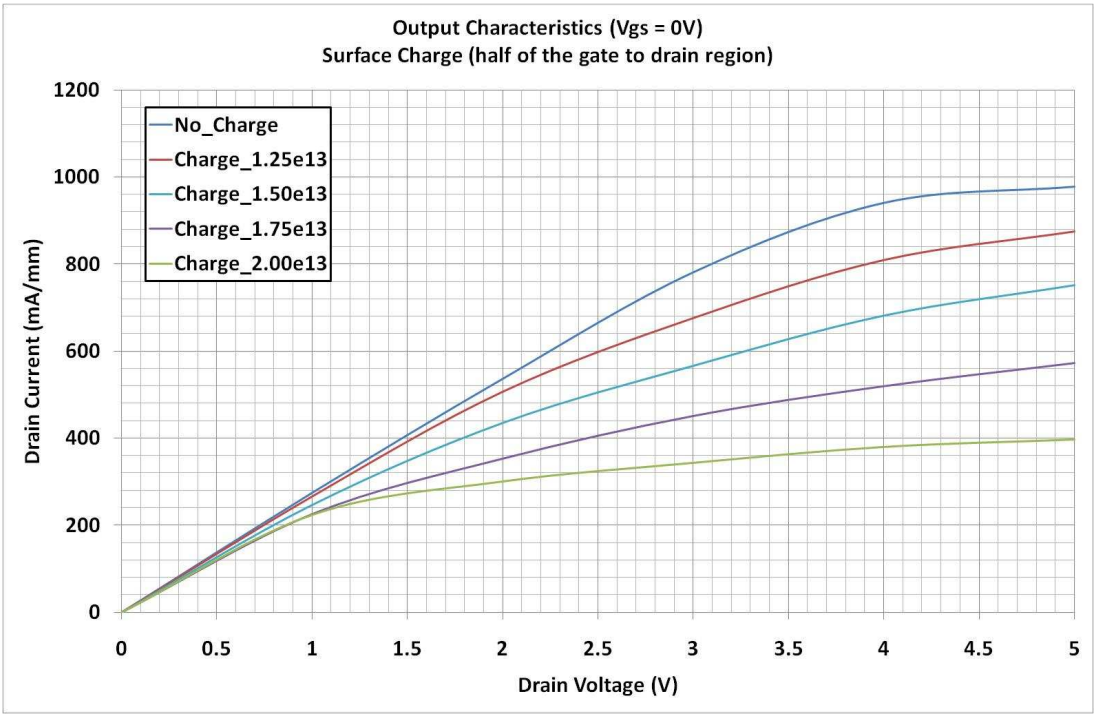

Figure 30: Output Characteristics (Vgs = 0V) for various surface charge densities (in cm^{-2}) over half the gate to drain distance.

Figure 30 clearly shows that for increasing charge on the surface of the device the degradation of the output current increases. This is due to the depleting of the electrons in the 2DEG due to the charging of the surface states in the GaN HEMT. This is clearly observed in Figure 31.

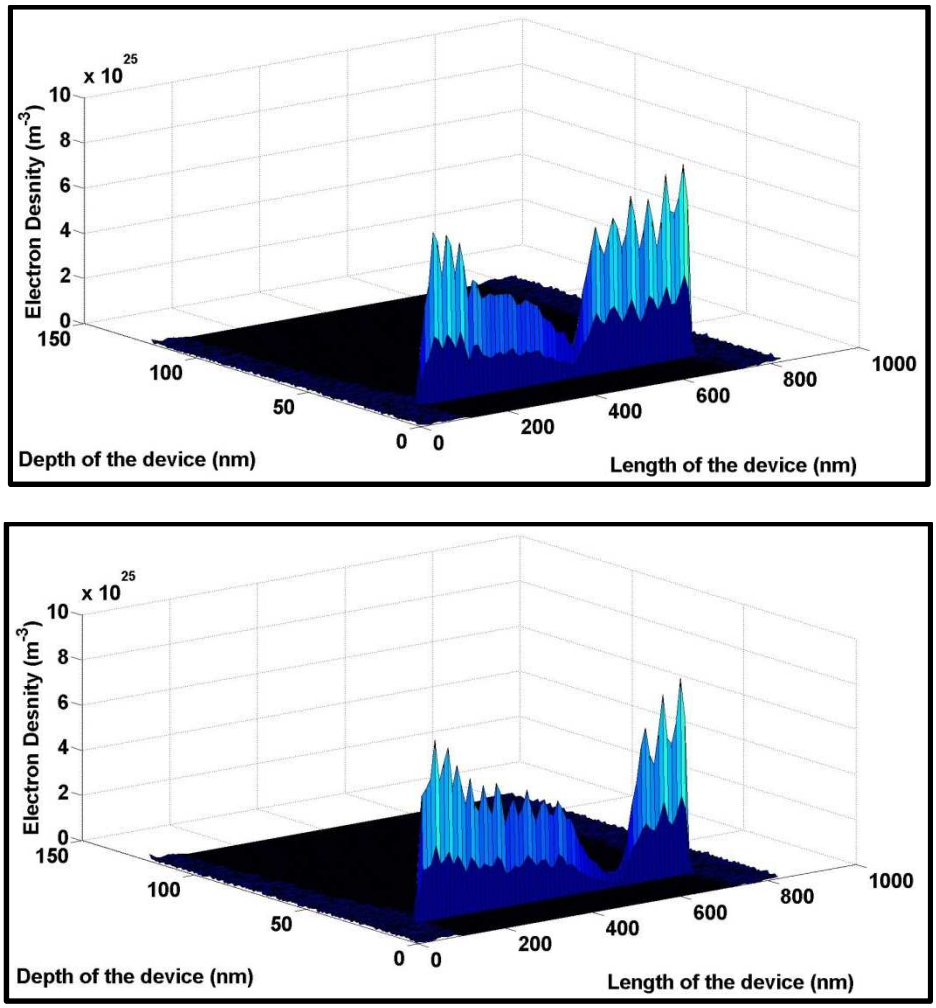

Figure 31: (Top) Electron density profile at Vgs = 0V and Vds = 5V with no charging of surface states

(Bottom) Electron density profile at Vgs = 0V and Vds = 5V with 1.5e13 cm^{-2} charge on the surface (over half the gate to drain extension region).

Figure 32 shows that when the surface states are charged for larger lengths above the gate to drain region the output characteristics of the device degrades further.

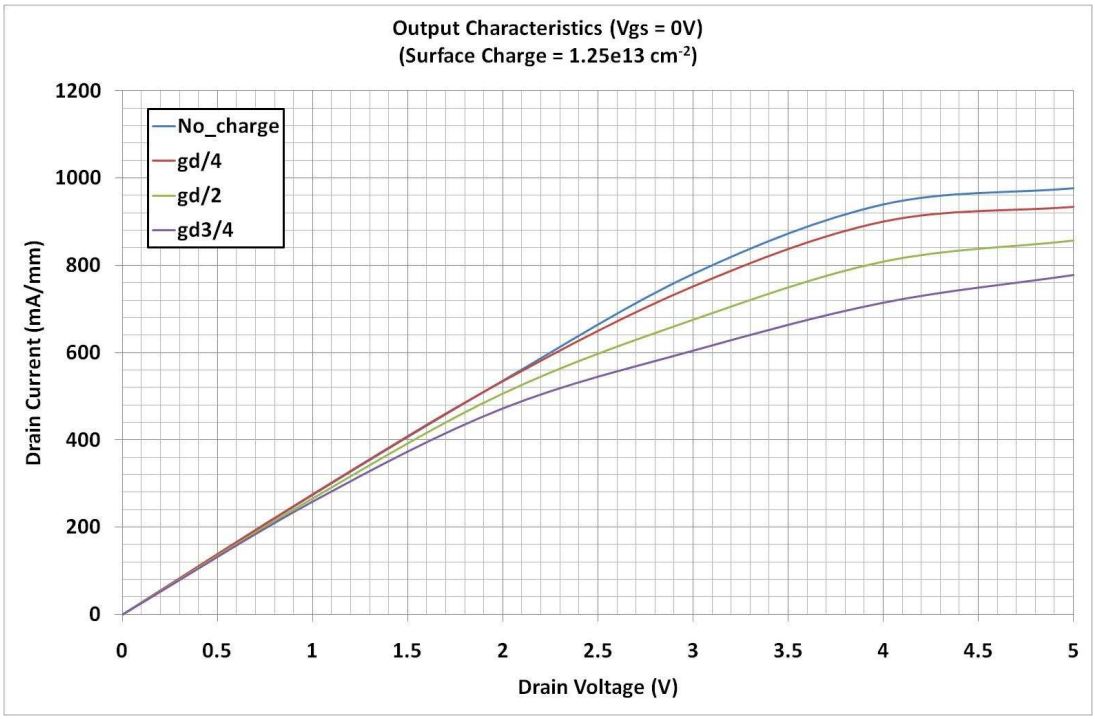

Figure 32: Output Characteristics (Vgs = 0V) for surface charge density of 1.25e13 cm^{-2} over various lengths of gate to drain regions.

Figure 33 shows the comparison of experimental data with simulations for surface state charging. In the experiment, the GaN HEMT device was stressed with DC bias and the output characteristics were measured before and after the stress. It is clearly seen that the output characteristics degrade significantly due to the charging of the defects in the AlGaN layer and surface traps [36].

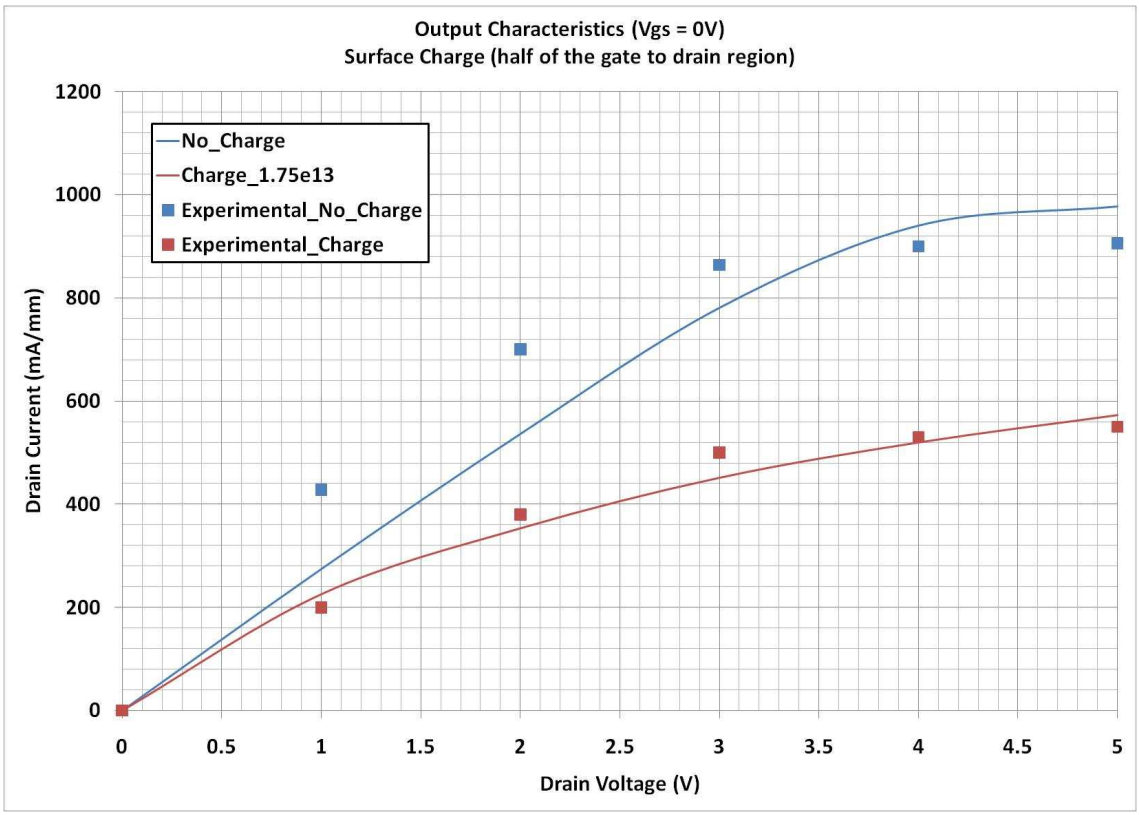

Figure 33: Comparison of Simulated output characteristics with experimental data for devices that have been stressed with DC bias.

Chapter 4

SHIELDING OF GaN HEMTs

I. SIMULATION RESULTS

In the previous work, it has been established that the gate-drain edge is very critical with regards to the reliability concerns seen in the GaN HEMT technology. One of the main reliability concerns as explained in the previous sections is the current collapse phenomenon due to self heating in these devices. This is attributed to the defects in the GaN layer and the interface between the passivation film and the AlGaN layer. The electron trapping in these defects is majorly influenced by the electric field at the gate edge, as shown in previous research studies [37]. In the present work, the effect of shielding the GaN HEMT structure on the thermal characteristics and the gate-edge electric field of the structure is being investigated.

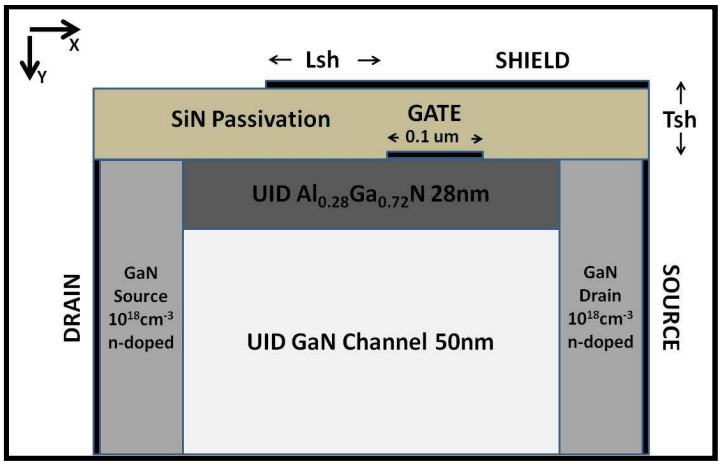

Figure 34: GaN HEMT structure with shield electrode

The device structure simulated for the evaluation of the influence of shield is shown in Figure 34. The shield (field plate) lengths and the shield dielectric thickness are varied to evaluate its influence on the thermal characteristics of the HEMT structure. The

shield length ‘Lsh” has been varied from 0.05µm to 0.4µm and the shield dielectric thickness, ‘Tsh’ has been varied from 20nm to 60nm.

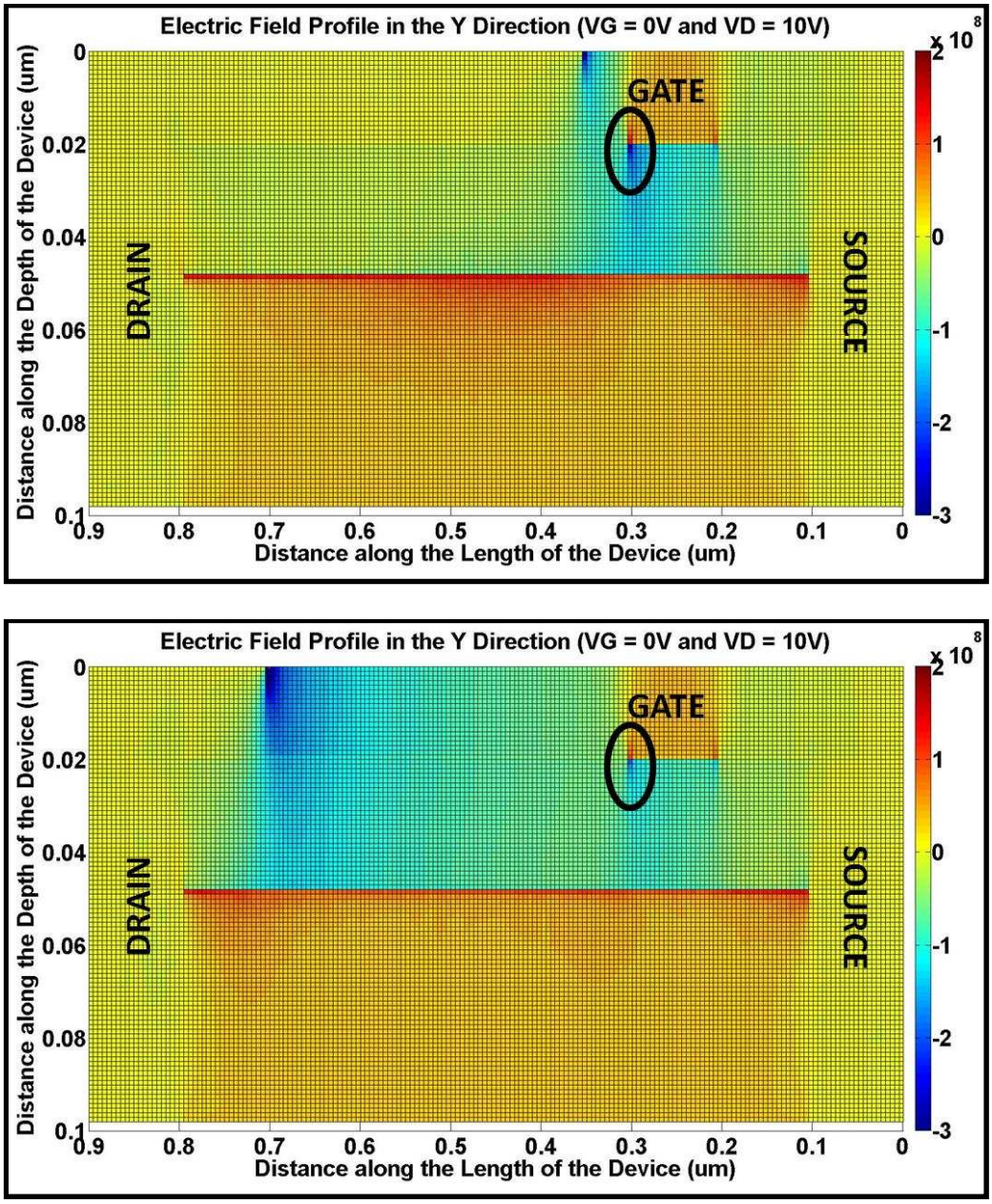

Figure 35: Electric field profile in the device with (Top) 0.05µm and (Bottom) 0.4µm shield lengths

The electric fields shown in Figure 35 shows that as the shield length increases, the electric field near the critical gate-drain edge reduces. This is because, as the shield electrode length increases, it spreads the electric field over a wider region. As the field near the gate-drain edge reduces, the potential for electron trapping in the defect sites also reduces and improves the reliability performance of the device structure. The electric field at the gate-drain edge varying with the shield lengths is clearly illustrated in Figure 36.

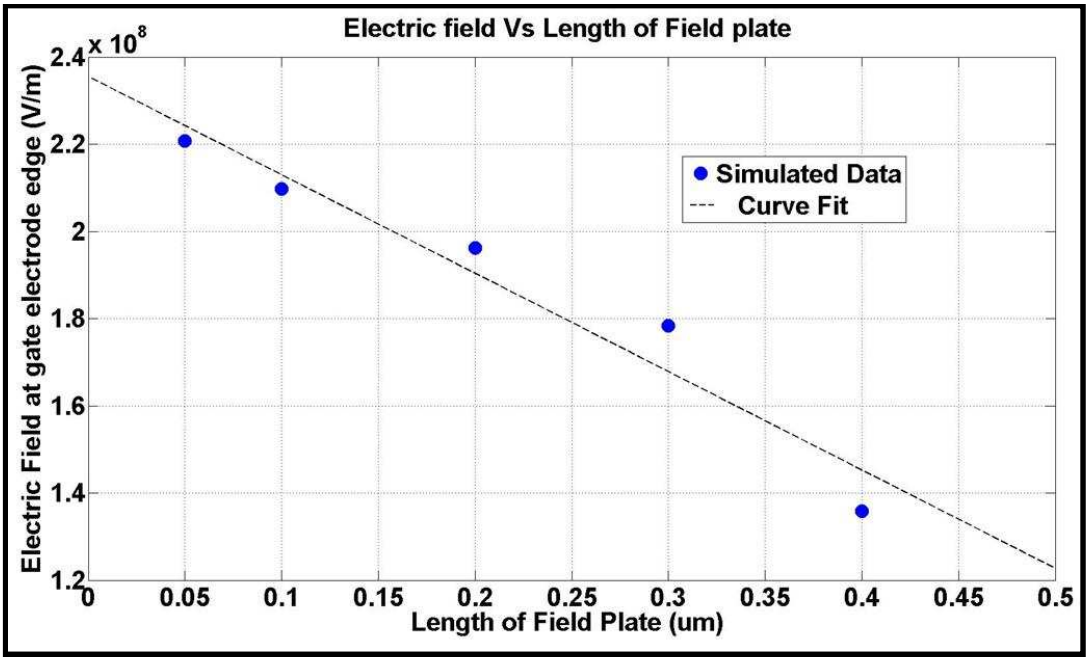

Figure 36: Vertical component of the electric field at the gate drain edge vs. field plate length

As the peak electric field moves far away from the gate-drain edge, the peak electron velocity also moves with it. The peak lattice temperature follows the peak electron velocity, as the energy of the electrons is highest in this region. This is clearly illustrated for various lengths of field plate in Figure 37.

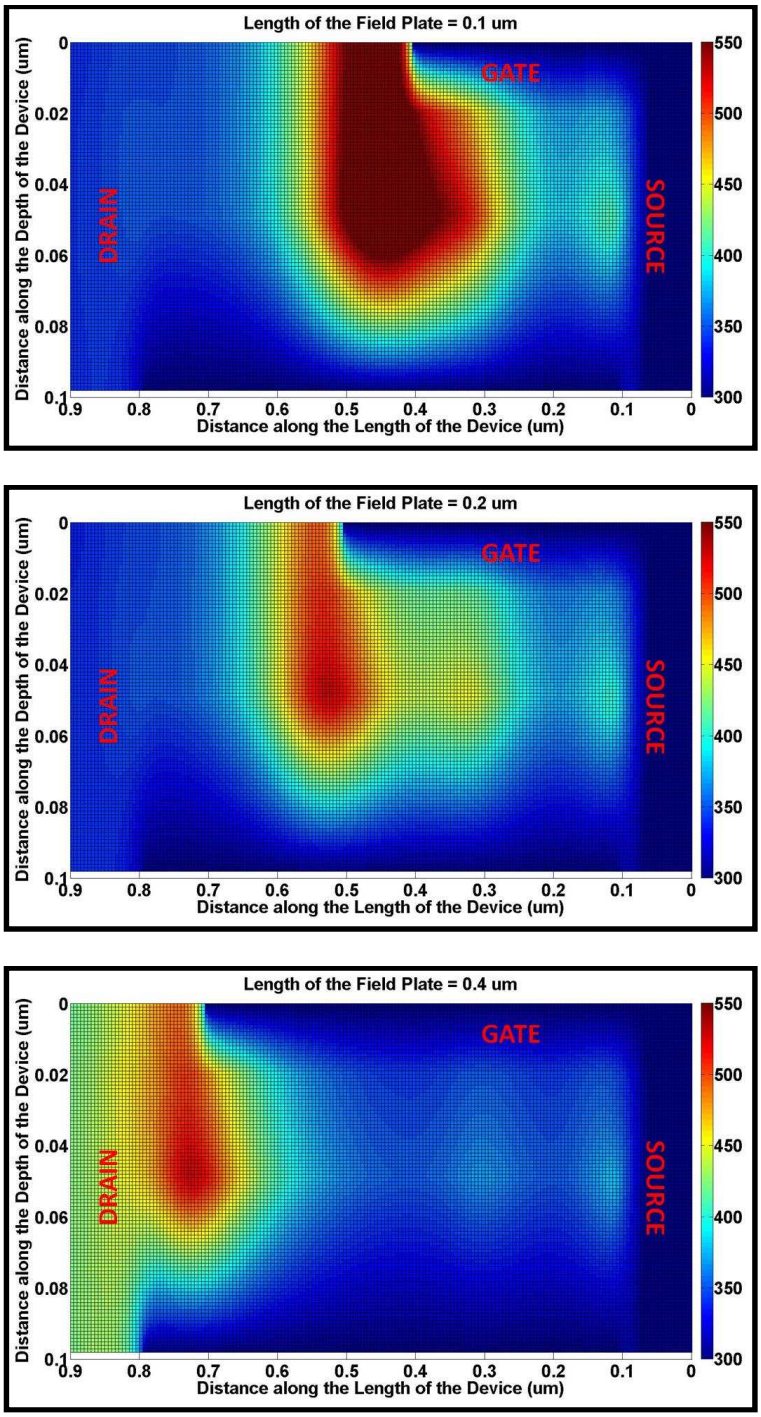

Figure 37: Lattice Temperature profiles in AlGaN/GaN HEMT for varying shield lengths

(Top) 0.1µm (Middle) 0.2µm (Bottom) 0.4µm

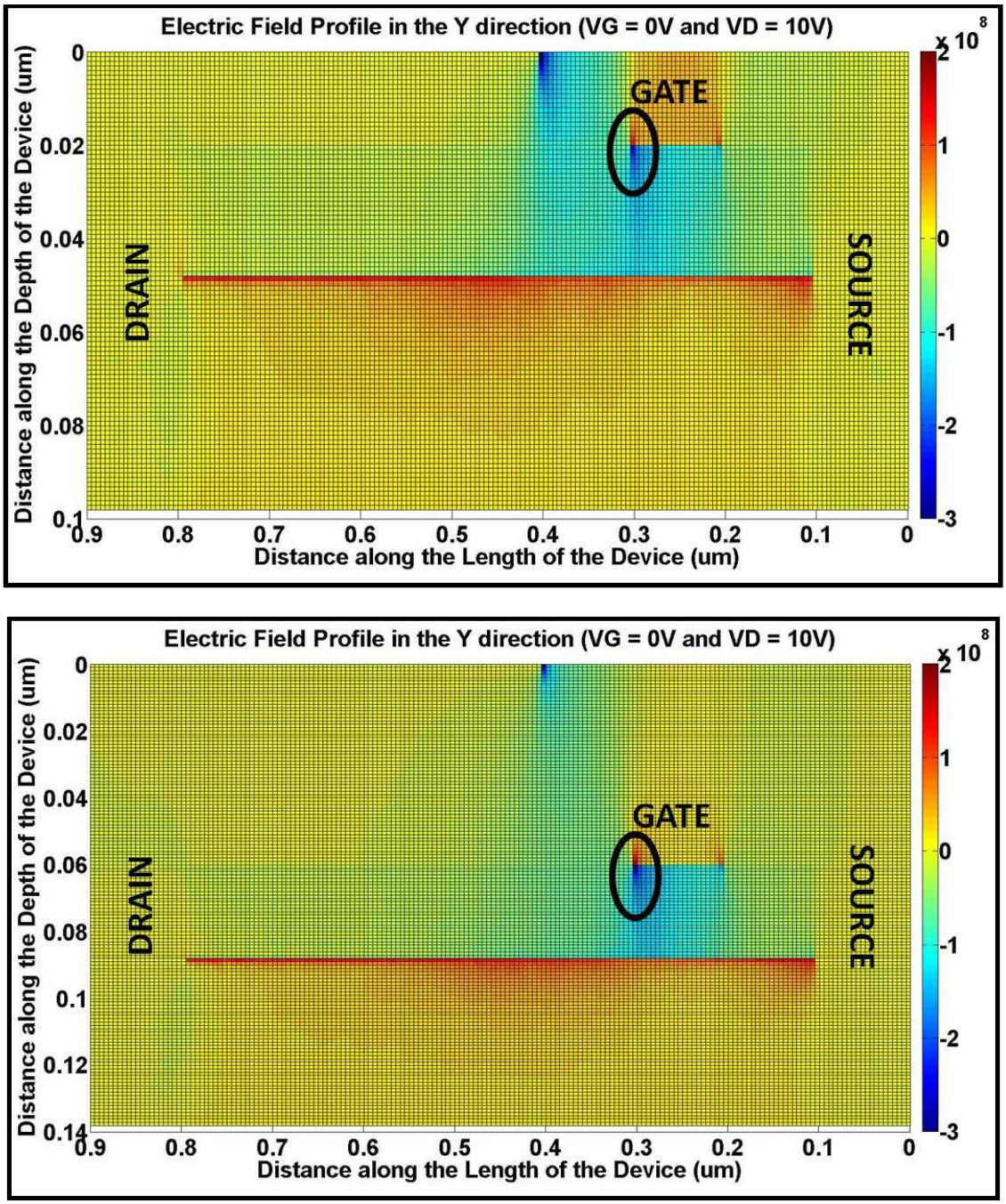

Figure 38: Electric field profile in the device for a shield length of 0.1µm (Top) 20nm and (Bottom) 60nm shield dielectric thickness.

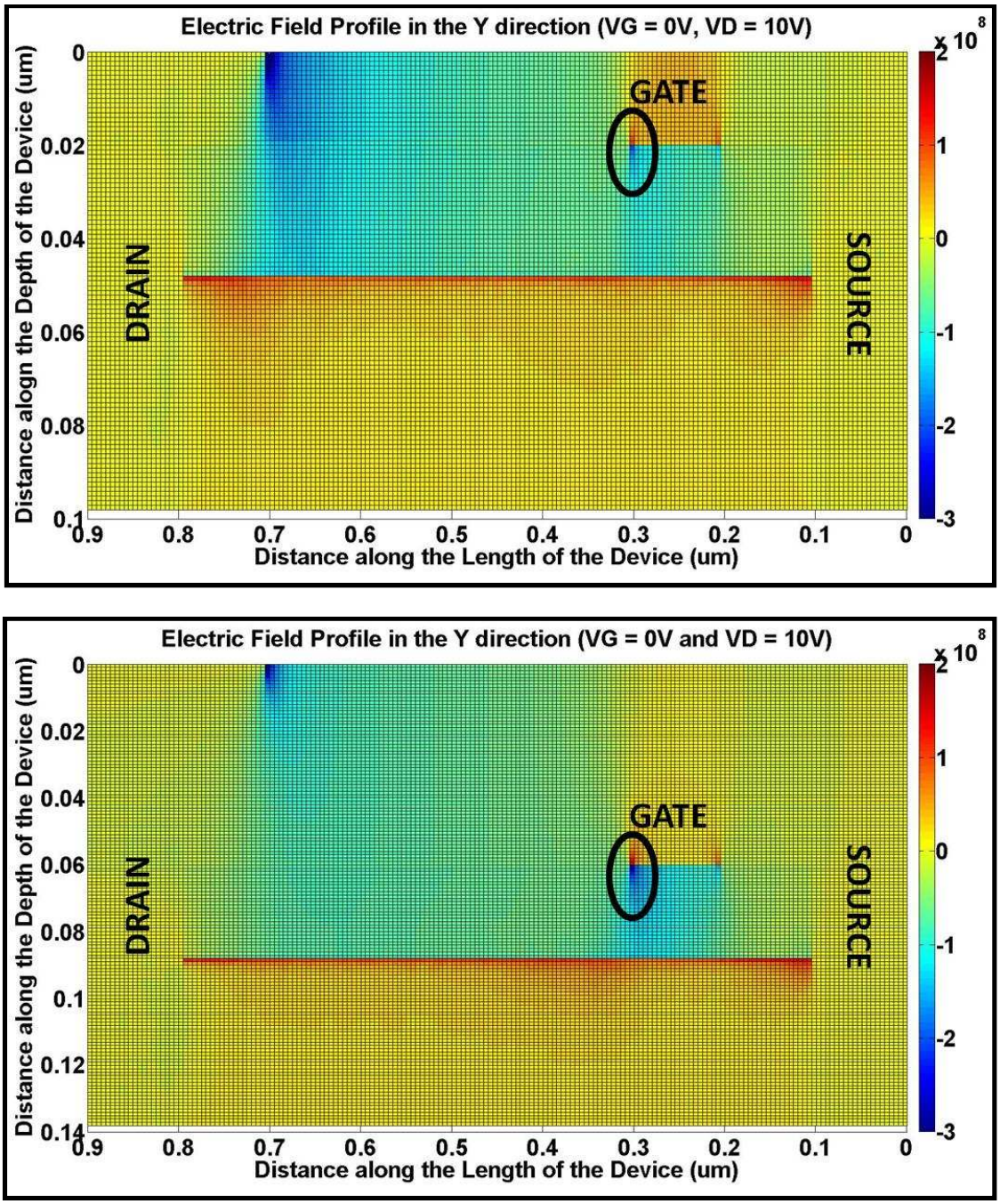

Figure 39: Electric field profile in the device for a shield length of 0.4µm (Top) 20nm and (Bottom) 60nm shield dielectric thickness.

The shield dielectric thickness is also varied for two different shield lengths. Its influence on the gate-edge electric field is similar to the effect of shield length. As the shield dielectric thickness increases, its ability to capacitively couple the electric field with the structure reduces. This results in increase of electric field near the gate drain edge. The effect of the shield dielectric thickness on the electric field profiles for two different shield lengths are shown in Figures 38 and 39. The electric field at the gate drain edge for varying shield dielectric thickness and shield lengths is shown in Figure 40.

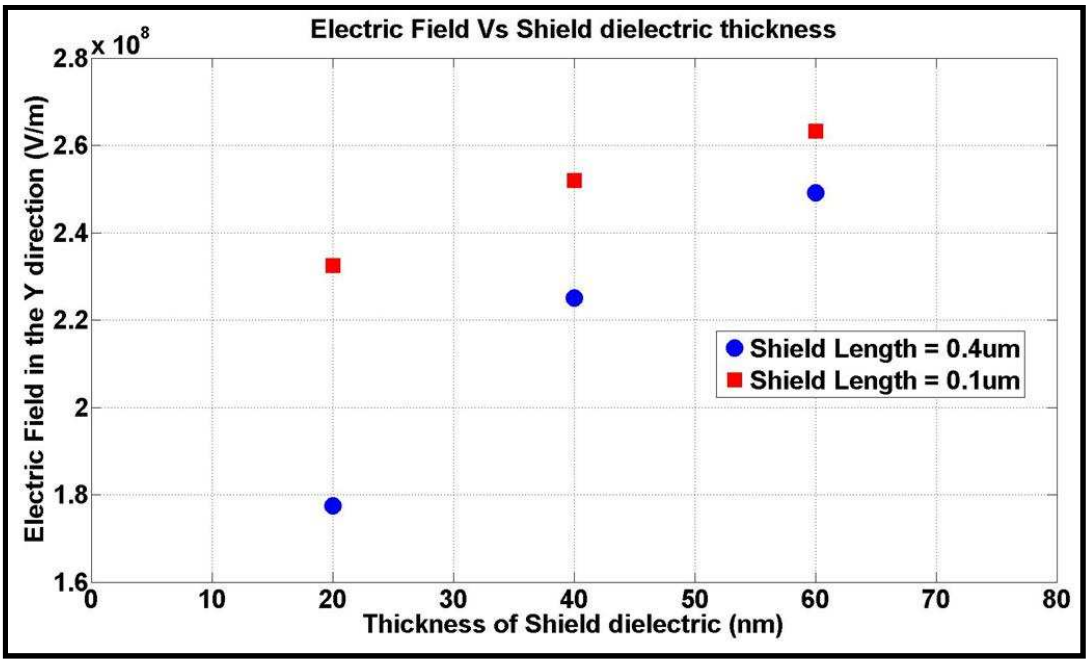

Figure 40: Vertical component of the electric field at the gate drain edge vs. shield dielectric thickness for varying shield length.

Chapter 5

BUCK CONVERTER

I. WORKING OF THE BUCK CONVERTER

GaN HEMT's operation, its reliability concerns and ways to reduce its impact on the performance of the device has been discussed in the previous chapters. The final part of the thesis is to study the application part of these power devices. One of the biggest markets for power MOSFETs is in the computing segment where they are generally used in buck converters (step-down converters). A simple circuit of such a synchronous buck converter is shown in Figure 41.

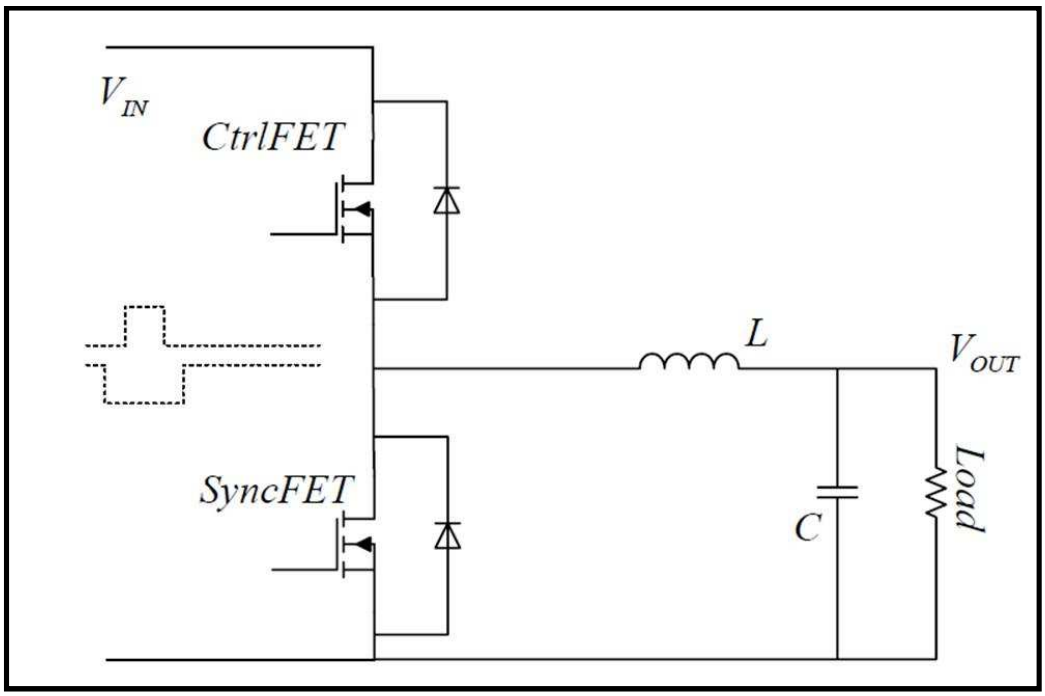

Figure 41: Synchronous Buck Converter [38]

It basically consists of two power MOSFET that are switched at a certain frequency (duty cycle) to obtain a certain Vout/Vin ratio. The output LC circuit acts as a low pass filter to stabilize the output voltage level. The functioning of the above circuit is

clearly demonstrated in Figure 42. It shows a state diagram that the buck converter goes through during its operation.

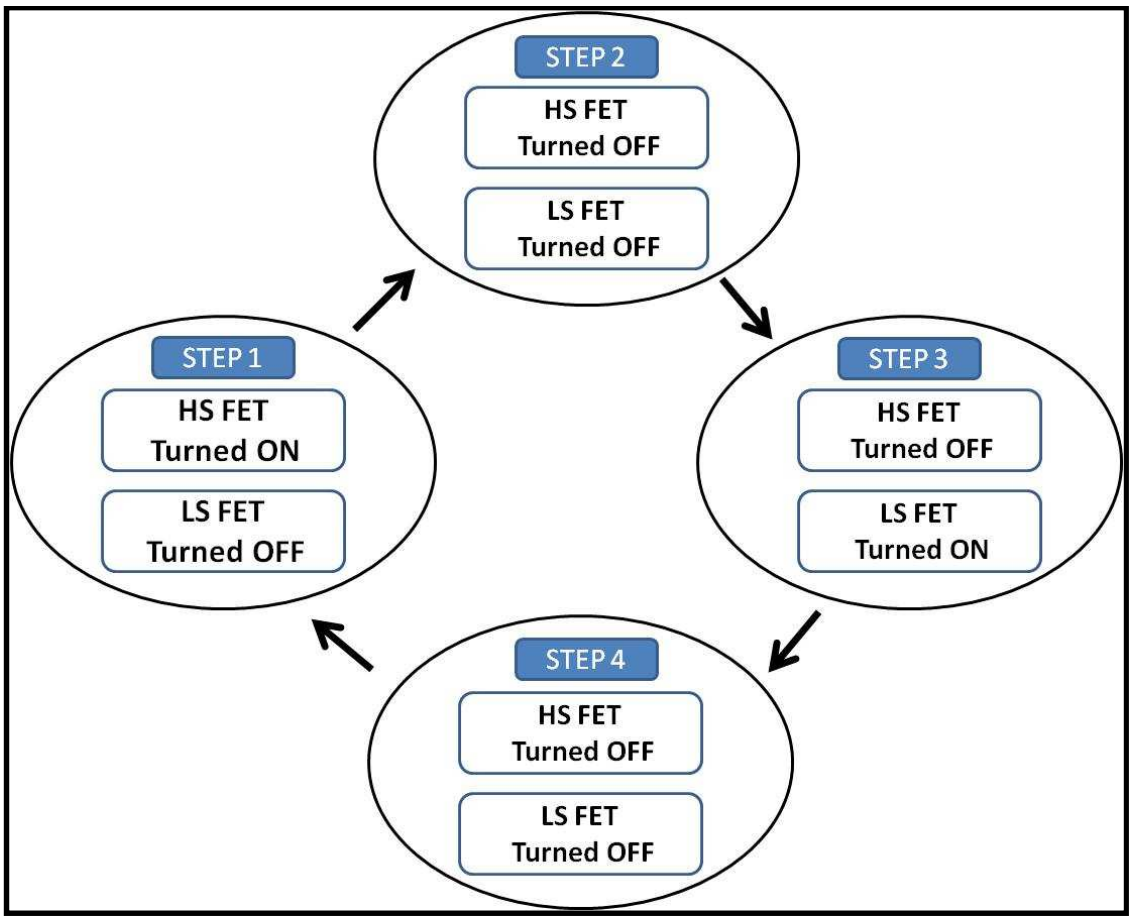

Figure 42: Synchronous Buck Converter flow chart

It basically consists of two power MOSFET that are switched at a certain frequency (duty cycle) to obtain a certain Vout/Vin ratio. The output LC circuit acts as a low pass filter to stabilize the output voltage level. A dead time is inserted between the switching of the gate signals of the CtrlFET and SyncFET so that both of them are not 'on' at the same time and cause a shoot-through. The functioning of the buck converter is as follows:

Step 1: The CtrlFET is turned on and the output inductor is charged from the supply voltage through the FET. During this step, the SyncFET is turned off and therefore is blocking a reverse voltage. The loss associated with this step is the conduction loss of CtrlFET.

Step 2: The CtrlFET is turned off and the SyncFET is also turned off as there is a dead time between their operations. The current for the output is provided by the body diode of the SyncFET. The dead time should be sufficient enough for the CtrlFET to turn off so that there is not a shoot through condition. This is a condition where both the SyncFET and CtrlFET are on and there is a direct shot to ground. This is a huge power loss. The dead time should not be too long as this is also a direct reduction in efficiency. Switching power loss of the CtrlFET and power loss in the body diode are the losses associated with this step.

Step 3: The current conduction transfers to the SyncFET and the output inductor sinks the current through the SyncFET. This FET is generally made to have a lower on resistance to prevent the current conduction loss as it is turned on for most of the time during a switching cycle. The power loss associated with this step is conduction loss of the SyncFET.

Step 4: The SyncFET conduction current is transferred to forward biased body diode. There is a dead time similar to Step 2 to prevent the shoot through condition. The current is then transferred from the body diode to the CtrlFET. During this time, the body diode goes from forward conduction to reverse bias. The power loss associated with this step is the reverse recovery loss.

Therefore, the losses associated with the operation of the buck converter are:

(a) CtrlFET conduction loss

(b) CtrlFET switching loss

(c) SyncFET conduction loss

(d) SyncFET switching loss

(e) Body diode loss

(f) Reverse recovery loss

II. POWER MOSFET

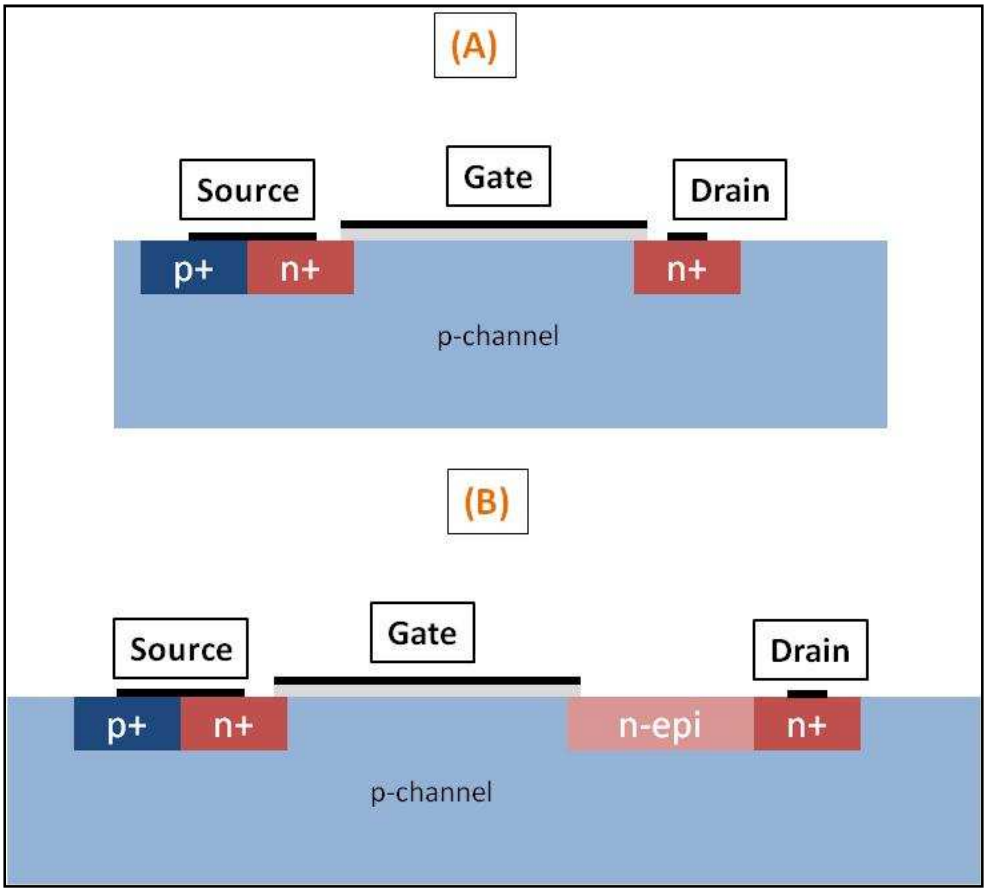

Figure 43: (A) MOSFET (B) Lateral Power MOSFET

Figure 43 (A) shows a basic MOSFET which operates with a low drain bias compared to a power MOSFET shown in (B). Power MOSFET is designed to have a very low resistance during the ON state of the device and blocks a very high voltage (on the drain) during the OFF state. Therefore, to hold a higher voltage and not breakdown the reverse diode, the voltage has to be spread across a larger region to keep the electric field under the critical breakdown electric field for Silicon. This is shown in Figure 43 (B) where an n-epi region is in the drain region to take a larger voltage in the drain region. This hurts the on resistance to a certain extent but helps in blocking a larger reverse voltage.

High voltage power MOSFET devices require a long n – epi region to support the voltage and the structure topology as shown in Figure 43 (B) takes up a lot of space on the wafer and are not very cost effective. This led to the development of vertical FET's in which the voltage was supported by an n-epi region, but vertically and would require a smaller space on the wafer as shown in Figure 44.

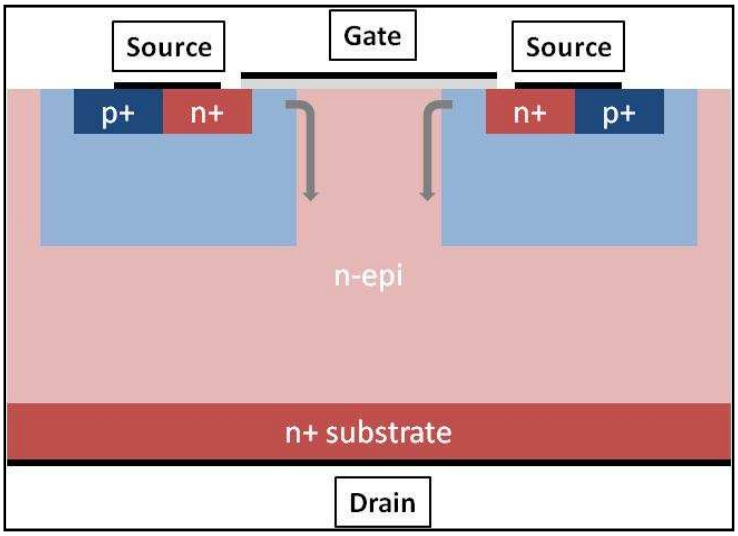

Figure 44: MOSFET with vertical topology

The structure in Figure 44 shows a power MOSFET with a lateral channel for current conduction and the drain electrode is the substrate contact. When the transistor is turned off and the drain voltage biases up to a large voltage, the n-epi/p junction takes the voltage and this makes the cell pitch (distance between two similar cells) on the wafer smaller. This design is very cost effective especially for high voltage devices.

To further improve the cell pitch of the device, power MOSFET with vertical channel was developed where the channel was vertical and the reverse voltage is also supported in the vertical fashion as shown in Figure 45.

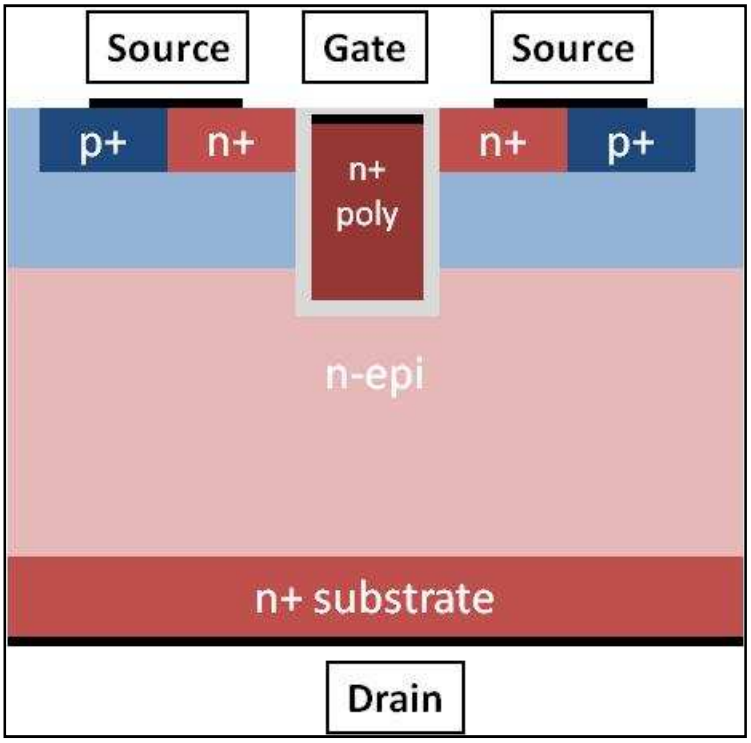

Figure 45: Trench Power MOSFET

III. POWER MOSFET PARAMETERS

The electrical parameters of power mosfet devices are:

(a) On resistance (Rdson)

(b) Breakdown Voltage (BVdss)

(c) Threshold Voltage (Vth)

(d) Gate Charge (Qg)

(e) Input Capacitance (Ciss)

(f) Transfer Capacitance (Crss)

(g) Output Capacitance (Coss)

On resistance (Rdson)

The Rdson of a device is split into various components:

$$Rdson = Rsource + Rch + Racc + Rdrift + Rsubstrate \quad (5.1)$$

Rsource = Source diffusion resistance

Rch = Channel resistance

Racc = Accumulation resistance

Rdrift = Drift region resistance

Rsubstrate = Substrate resistance

When the device is operated with a lower gate voltage, the on resistance of the device is dominated by the channel resistance. In the operation of the device with a higher gate voltage, the channel is in very strong inversion reducing the channel resistance significantly. In this region of operation, the drift region resistance is the dominating resistance.

Similarly, for a low voltage power MOSFET the n-epi region can be highly doped as it does not have to support a large voltage and therefore the channel resistance dominates the Rdson of the device. On the other hand in a high voltage power MOSFET, the n-epi region is very low doped to support a large voltage and therefore the drift region resistance dominates.

Breakdown Voltage (BVdss)

Breakdown voltage is the voltage at which the reverse biased diode has a significant amount of current flowing through it due to the avalanche multiplication process. Both the gate and source electrodes are short to ground during this operation of the device. As explain in the previous sections, the voltage is supported by a p/n-epi junction and higher the voltage, lower the doping of the n-epi region. Almost all the voltage is taken by the n-epi region, but the p-channel also depletes to a certain extent. This should be considered in the design of the power MOSFET so that there is no punch-through effect, where the depletion region in the channel reaches the source and forms a short from drain to source.

Threshold Voltage (Vth)

The gate voltage at which the channel inverts and starts conducting current from drain to source is threshold voltage. Generally, in the industry it is specified as the gate voltage at which the drain current is 250uA.

Capacitances

Ciss (Input capacitance), Crss (Transfer capacitance) and Coss (Output capacitance) are the three main capacitances in power MOSFETs.

$$Ciss = Cgs + Cgd \tag{5.2}$$

$$Crss = Cgd \tag{5.3}$$

$$Coss = Cds + Cgd \tag{5.4}$$

The transfer capacitance (Crss) is a very important parameter because it is in a feedback loop between the input and the output of the circuit. It transfers as a miller capacitance both in the input and the output circuit.

The input capacitance (Ciss) is an important parameter for the turn on of the device. The larger the capacitance, the more time it takes to charge it and turn on the device. Therefore, it is ideal to keep this capacitance low to have a good figure of merit for the device.

The output capacitance (Coss) is an important parameter during the switching of the device from turn off to turn on since this capacitor has to be discharged in the process.

Gate Charge (Qg)

Gate charge, shown in Figure 46 is the most important parameter for the switching characteristics of the device. When the gate is connected to the supply voltage, the current initially flows to charge Cgs. After Cgs is completely charged and the drain current reaches the predetermined current Id and stays constant while the drain voltage falls. The Vgs becomes constant and the drive current starts to charge Cgd. After Cgd is charged, the gate voltage starts rising again.

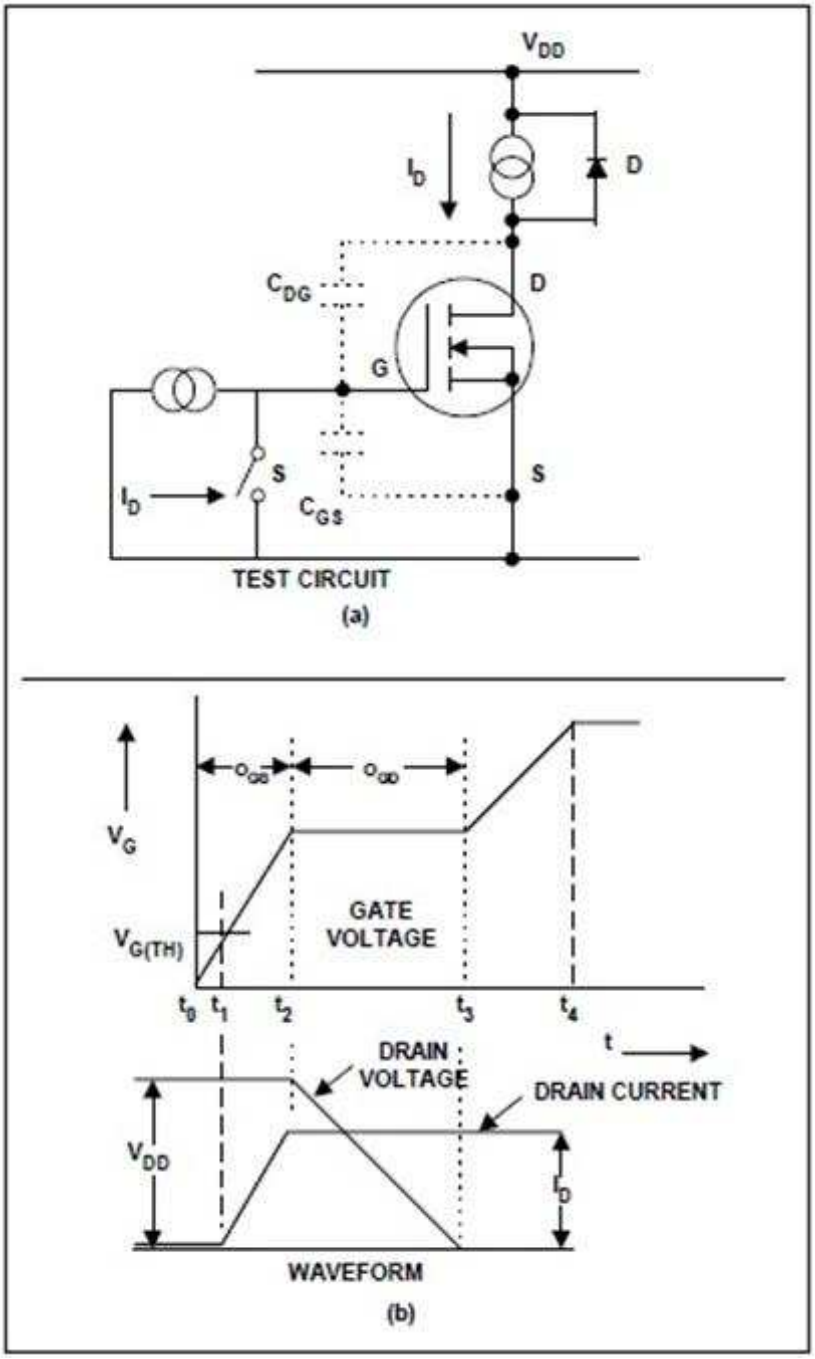

Figure 46: Gate Charge Circuit [39]

IV. TRENCH POWER MOSFET

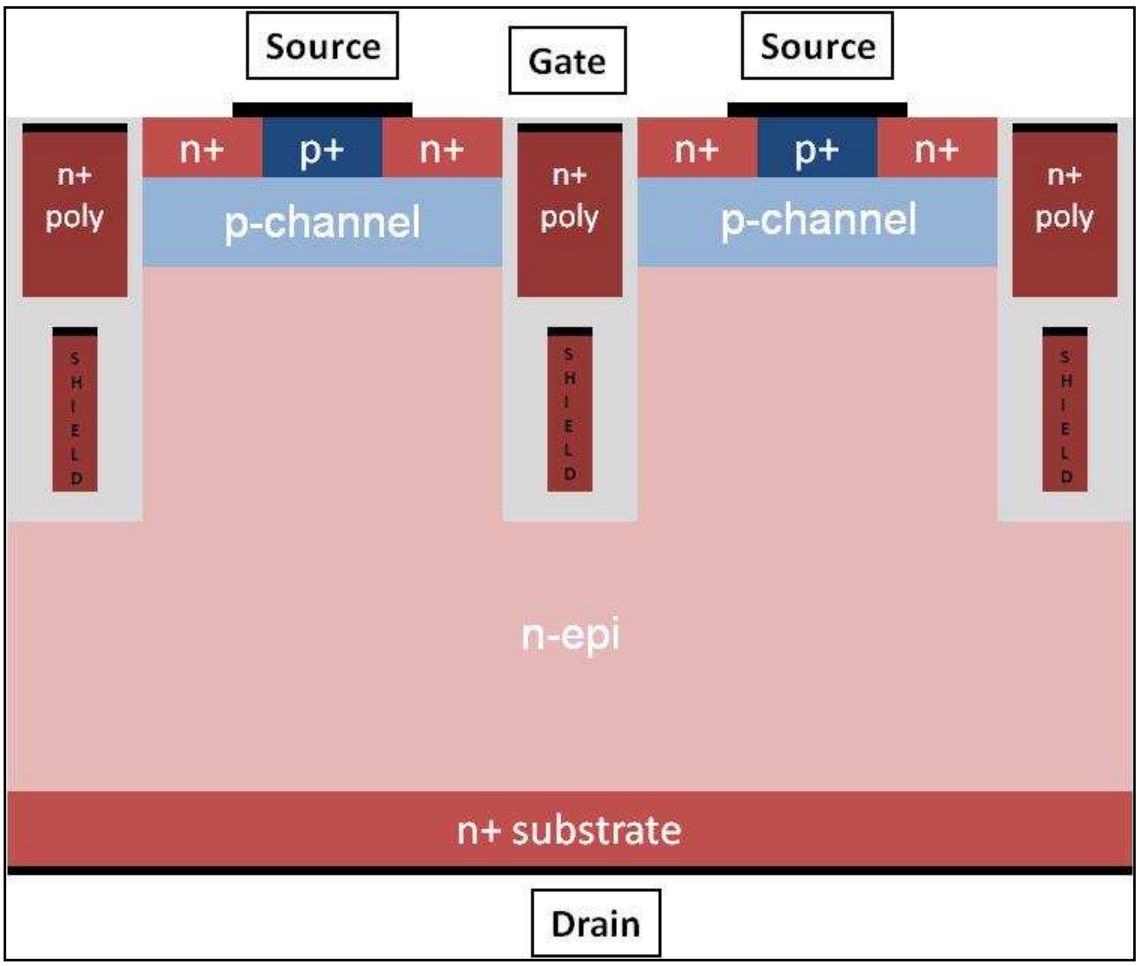

Figure 47: Shielded Trench Power MOSFET

The Trench power MOSFET shown in Figure 47 is similar to the device structure in Figure 45 and the device operation is similar. The channel is vertical in this structure and the voltage is also supported by the n-epi vertically. The major improvement in this structure is the shielding of the device. The shield acts like a MOS capacitor and helps in depleting the n-epi region and reduces the electric field near the p-channel/n-epi junction. The presence of shield in the device structure improves the performance of the device n a couple of ways:

(a) It helps in doping the n-epi region higher for a given breakdown voltage as the shield electrodes help in supporting the voltage from both directions in a cell in addition to the p-channel/n-epi junction.

(b) The transfer capacitance (Crss) / miller capacitance of the device is one of the most important parameter of the device. This capacitance reduces in a non linear fashion with the increase in reverse drain voltage as the n-epi region gets depleted. The presence of shield makes the gate to drain capacitance of the device roll of faster with drain voltage as the region near the p-channel/n-epi junction gets depleted quickly.

The gate charge of the device is mainly dependent on the channel length, gate-drain overlap and gate-source overlap of the device.

V. BUCK CONVERTER SIMULATION RESULTS

A mixed mode simulator was developed using Sentaurus TCAD for simulating the buck converter application circuit as shown in Figure 48. The devices (SyncFET and CtrlFET) used in the simulation are Trench Power MOSFET similar to structure shown in Figure 47 generated using TCAD process simulators.

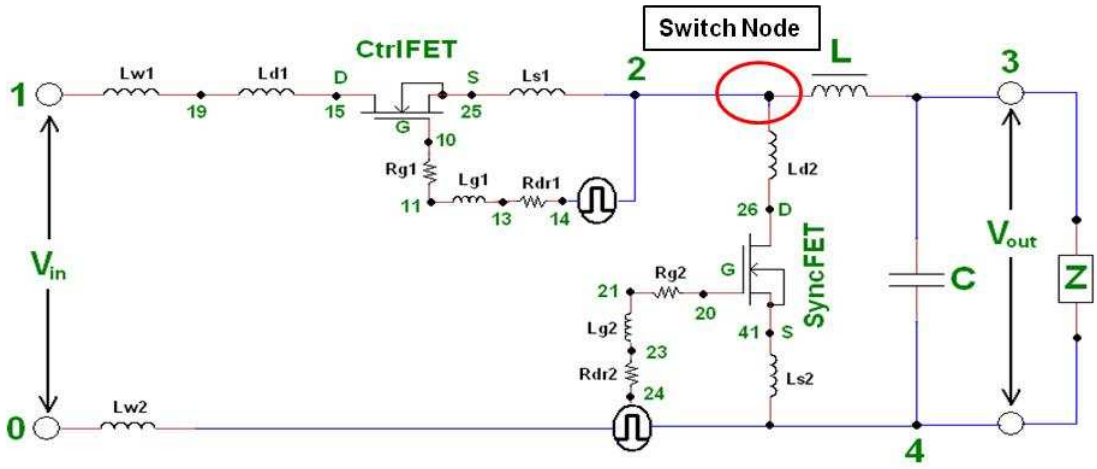

Figure 48: Simulated Buck Converter Circuit

The circuit consists of several parasitic components:

Lw1, Lw2 – Trance wire inductances

Ld1, Ld2 – Package drain inductances

Ls1, Ls2 – Package source inductances

Lg1, Lg2 – Gate inductances

Rg1, Rg2 – Gate resistances

Rdr1, Rdr2 – Driver resistances

L, C, Z – Load inductance, capacitance and impedance

The simulation has been run for frequencies of 300 KHz, 500 KHz, 700 KHz and 1000 KHz and for various output currents ranging from 0-25A. The efficiency Vs Output

current for various frequencies and the waveforms from simulations have been compared to application measurement (Apps) data.

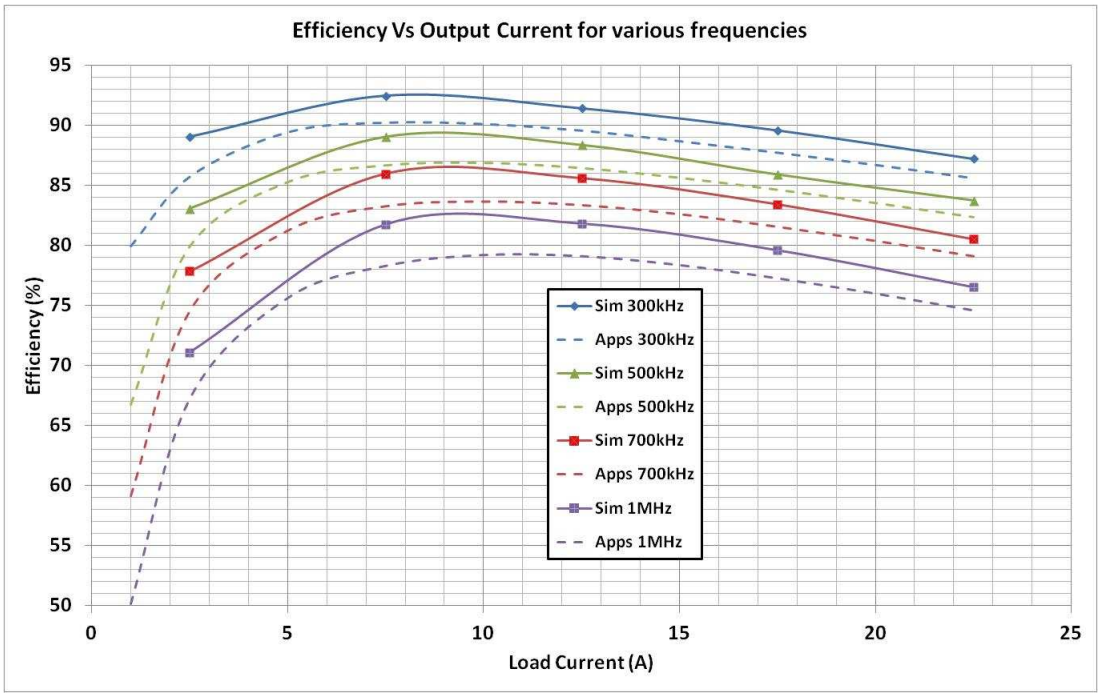

Figure 49: Buck converter efficiency vs. Output current

The results of the buck converter simulation presented in Figure 45 clearly shows 9that as the output load current of the circuit increases, the efficiency of the curve increases to a peak value and then starts decreasing for higher load currents. At lower load currents, the switching loss of the device dominated which reduce the efficiency and at higher load currents the conduction current losses of the device dominate and reduce the efficiency. The SyncFET reverse recovery losses also reduce significantly with the increase in output load current. This is clearly shown in Figure 50.

Figure 49 shows that, as the frequency of the operation is increased from 300 KHz to 1 MHz, the overall efficiency across all load currents reduces significantly (~ 10%).

This is because as the frequency is increased the switching loss of the device increases. This is clearly observed from the differences between Figures 50 and 51.

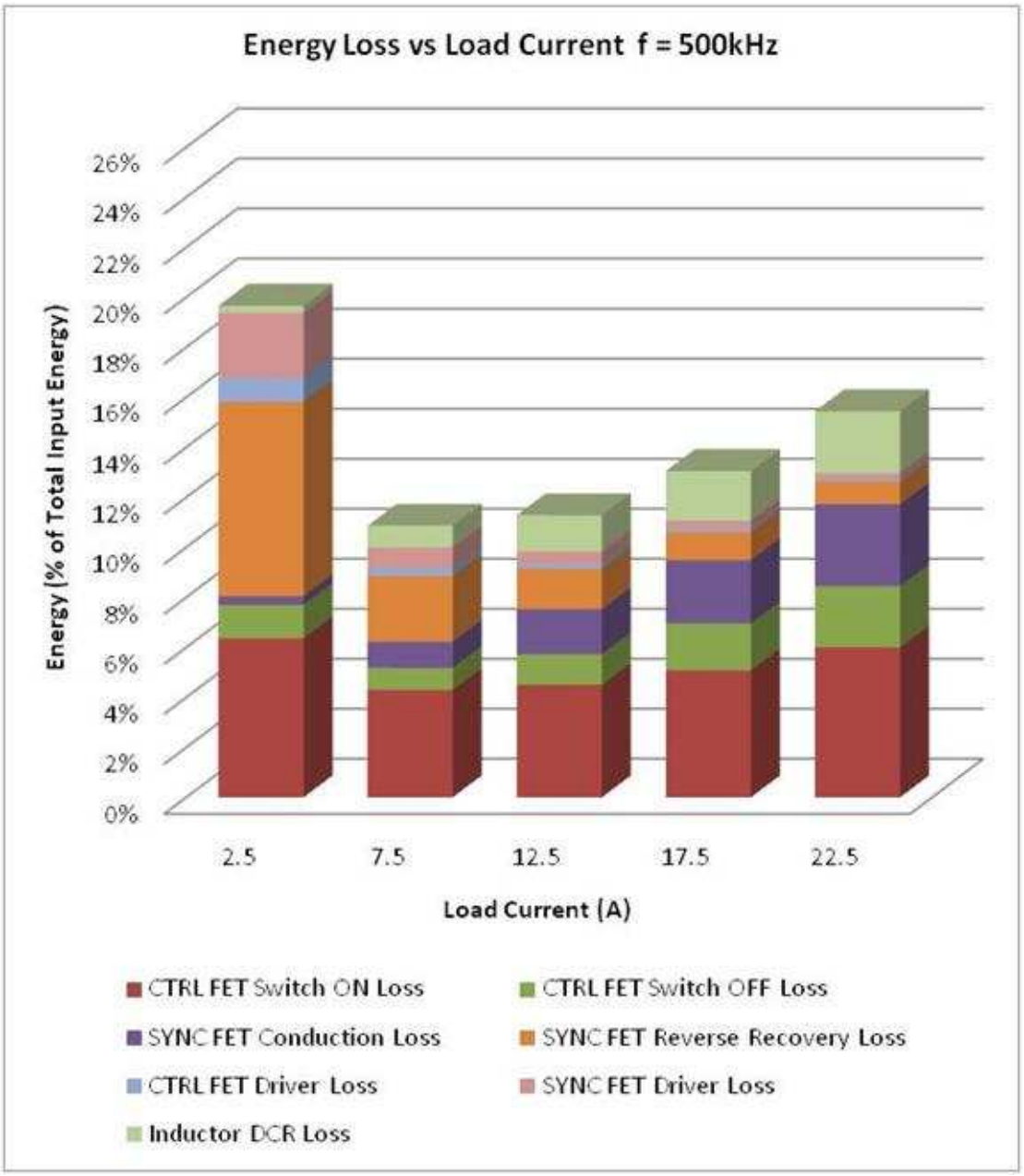

Figure 50: Energy loss breakup at 500 KHz

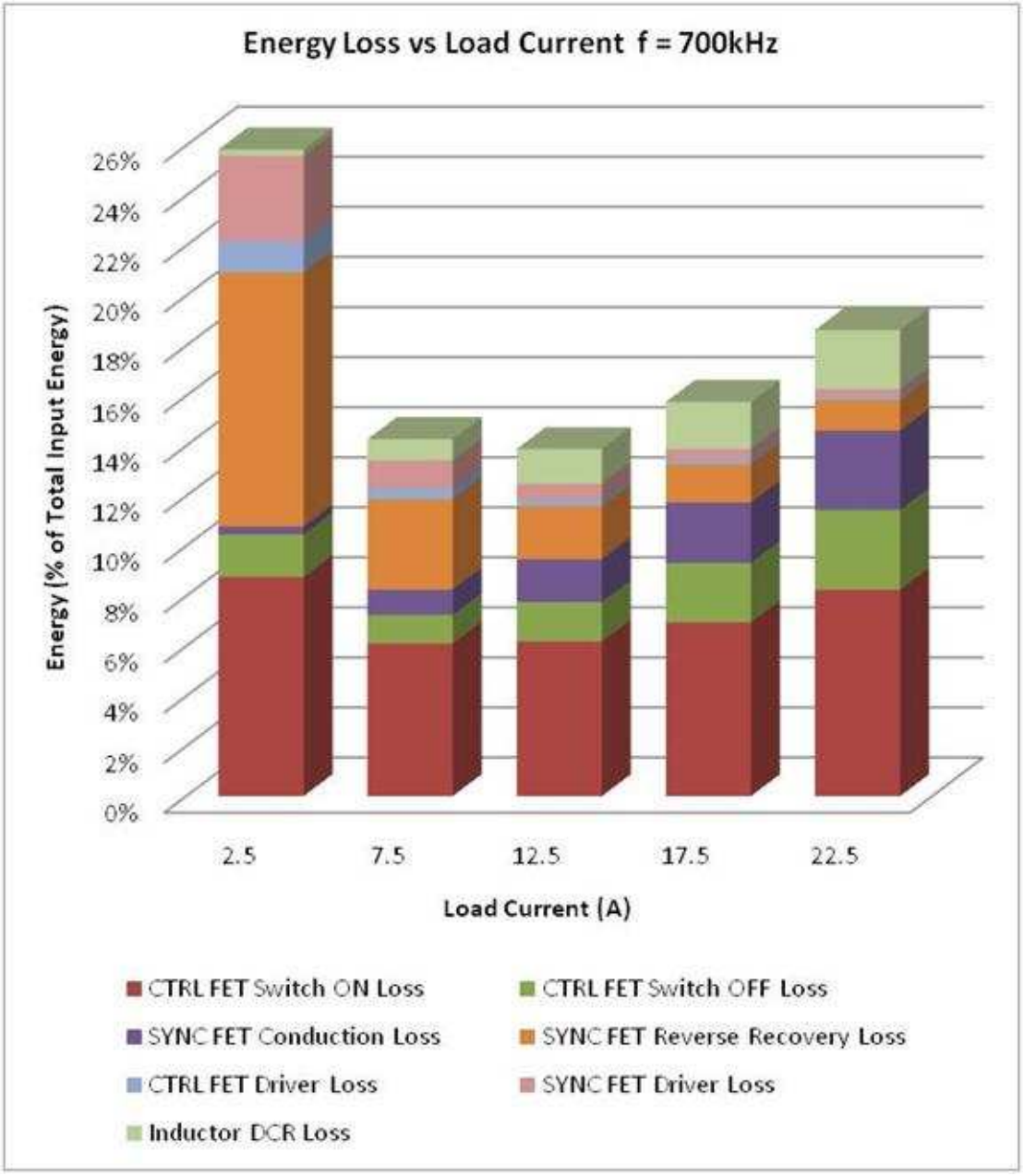

Figure 51: Energy loss breakup at 700 KHz

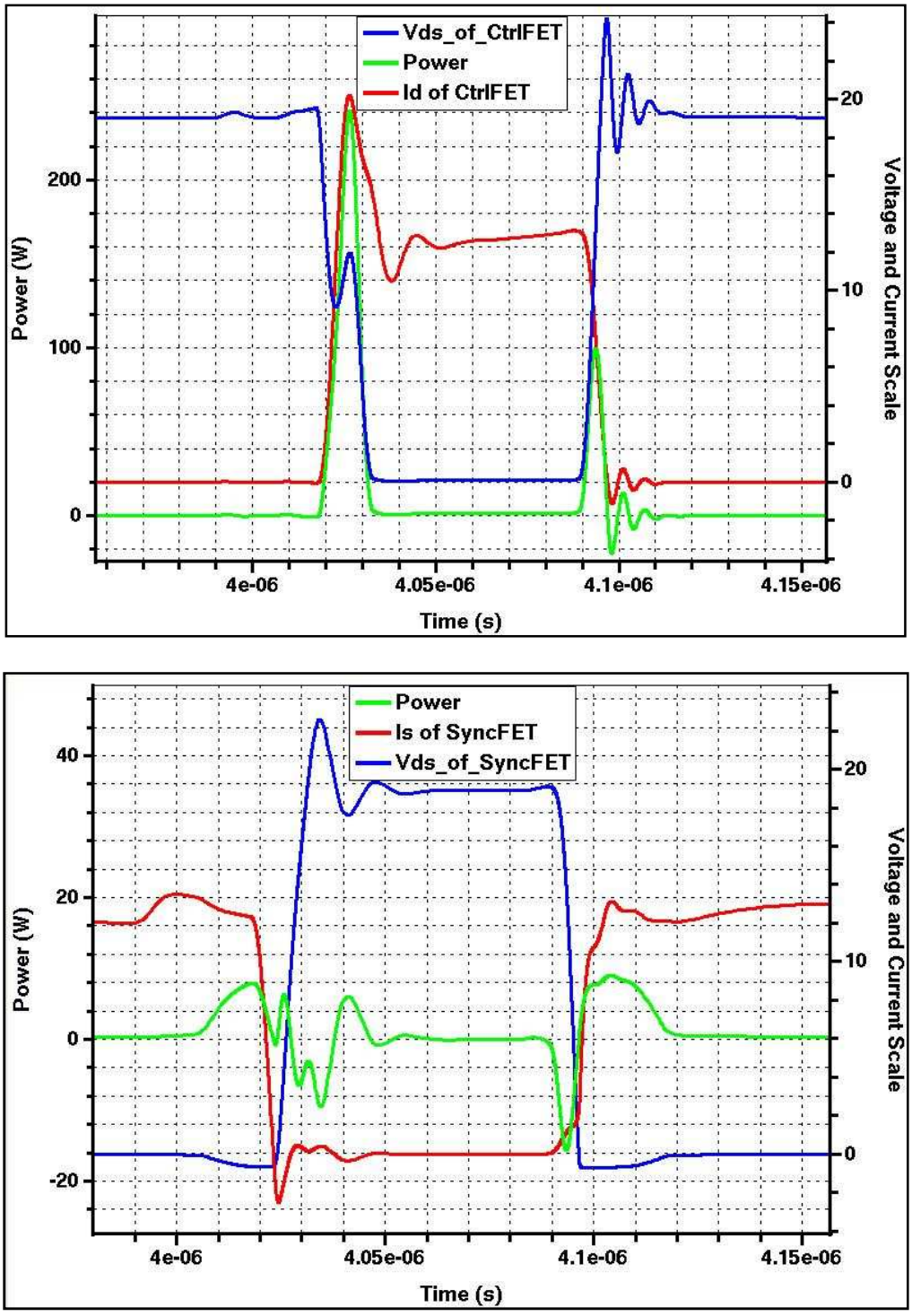

Figure 52: Switching waveform of (Top) CtrlFET (Bottom) SyncFET

When the CtrlFET in the circuit shown in Figure 48 turns on, the switch node (source side of the CtrlFET) is railed to the supply voltage and the drain to source voltage across the CtrlFET goes to zero as shown in the top panel of Figure 52. The blue curve (Vds across the CtrlFET) goes to zero and when it switches from zero to a higher voltage, the switching losses come into play. This is shown by the green curve which spikes up during the transitions in the voltage and current. The value of power is non zero between the switching times and contributes to the conduction loss of the CtrlFET. This is a smaller percentage when compared to the switching losses as the FET is turned off for the most part in a duty cycle.

The switching loss of the CtrlFET strongly depends on the gate charge of the device which directly depends on the input capacitance (Ciss) of the device. The other parameter of the device that the switching loss of the device depends on is the output capacitance (Coss) of the device which has to be charged and discharged every switching cycle. The Rdson of the device which contributes to the conduction loss of the device is not as important as gate charge for the CtrlFET as the switching losses are more dominant.

When the SyncFET in the circuit shown in Figure 48 turns on, the switch node (drain side of the SyncFET) is railed to the ground voltage as shown in the bottom panel of Figure 48. When the CtrlFET turns off, the SyncFET diode turns on and provides the current for the output LC circuit. The drain to source voltage across the device when the diode is conducting is around 0.7-1.0V. This current is switched from the diode to the SyncFET towards the end of the dead time cycle and the Vds across the device goes closer to zero. Similarly, when the SyncFET is turning off, the current switches from the

FET to the reverse recovery current of the SyncFET diode which is provided by the CtrlFET turn on. The drain to source voltage across the SyncFET goes from close to zero to the supply voltage during this cycle.

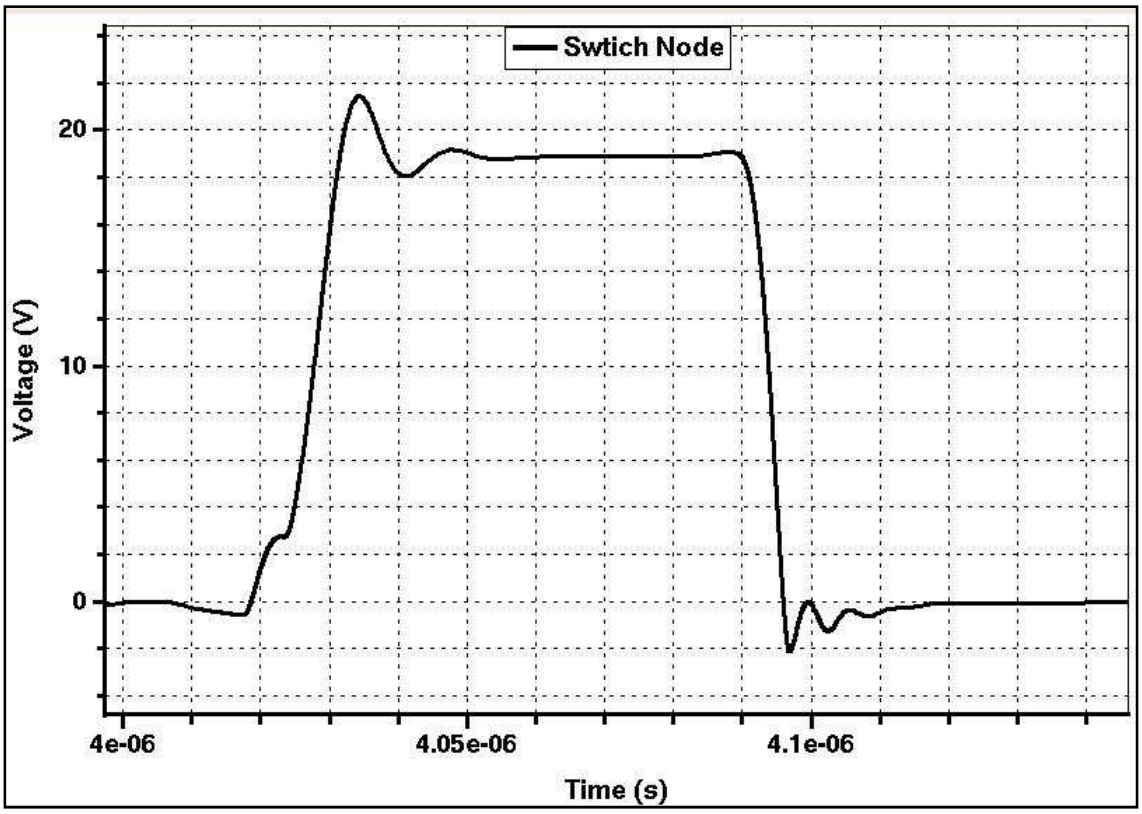

Figure 53: Switch Node waveform

The switching loss of the SyncFET is lower compared to the CtrlFET as observed from Figure 52 since the voltage switching across the device is from 0.7V to 0V. The conduction loss of the SyncFET is a larger component of the loss as it is switched on for the most part of a duty cycle. This loss mechanism strongly depends on the Rdson of the device and therefore has to be made lower for higher efficiency. The other loss mechanism in a SyncFET is the reverse recovery loss of the inherent diode in the device. This has to be kept lower for a higher efficiency of the buck converter application. The

switch node waveform of the buck converter circuit shown in Figure 48 is shown in Figure 53.

VI. GaN HEMT For Buck Converter

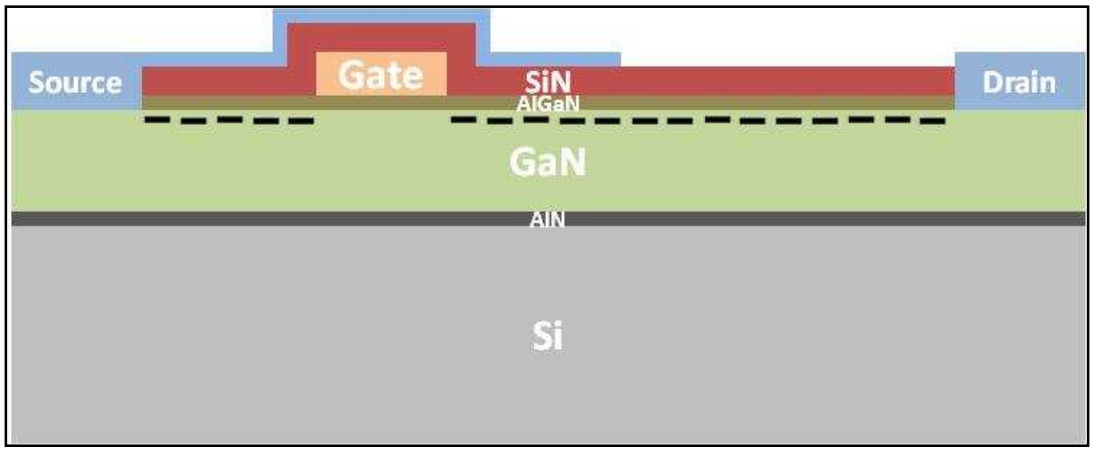

Figure 54: GaN HEMT [40]

The major advantage of the GaN HEMT compared to the Silicon Power MOSFET is that as the GaN material is highly piezoelectric in nature and higher band gap, the 2DEG is high resulting in a low Rdson for a high voltage device. The temperature coefficient of Rdson for a GaN HEMT device is positive and is similar to a Silicon MOSFET device but the temperature coefficient is significantly lower for the GaN FET. This results in GaN FETs having lower conduction loss for technologies with higher breakdown voltage compared to Silicon FETs.The GaN FET is a lateral device and therefore the gate to drain capacitance is lower has a better process control compared to a vertical FET. The input capacitance which is mainly influenced by the channel length is also lower and can be controlled better during processing for a lateral device in comparison to a vertical device. Lower capacitance results in lower gate charge and therefore reduces the switching losses in the device significantly. This also results in the

operation of the buck converter in high frequency applications with good efficiency compared to Silicon Power MOSFETs.

The other main advantage of the GaN FETs compared to Silicon FETs is the absence of the body diode. The reverse bias or body diode operation mechanism in GaN FETs is very different compared to Silicon FETs. Assuming that the FET shown in Figure 54 is an enhancement mode device, with zero bias on the gate, there is no channel under the gate and the device is turned off. When the drain voltage of the device starts falling, a positive bias on the gate is created relative to the drift region which injects electrons into the channel and starts conduction. This eliminated the minority carrier conduction involved in the reverse recovery mechanism of a silicon diode and therefore the Qrr (reverse recovery charge) in a GaN FET is zero. This also improves the switching characteristic and the efficiency of the circuit especially under high frequency conditions. However, the output capacitance (Coss) does exist in the GaN FET between the shield (Source) and the drift region (drain side) of the device. This has to be charged and discharged every cycle and therefore the design of this capacitance is more critical in GaN FETs. In Silicon devices the shielding helps in improving the breakdown characteristics of the device without sacrificing much of the Rdson of the structure. However, in GaN FETs the presence of shield not only improves the breakdown characteristics of the device but plays a key part in improving the reliability performance of the device. It helps in keeping the electric field low especially in the gate to drain edge and reduces the dynamic Rdson resulting from current collapse in the device.

Chapter 6

CONCLUSIONS

In conclusion, this work has been done to understand the reliability concerns in GaN HEMT technology and some methods to reduce its impact on the performance of the device. In this process, the following milestones were completed:

A theoretical model which provides the gate voltage dependence of the piezoelectric polarization charge in the GaN HEMT devices. This simple model utilizes a generalization of Gauss's law, imposing constraints on the electric displacement vector D. The constraint on D is given by the continuity of the perpendicular component of the displacement across an interface. Poisson's equation is then solved across various layers under proper boundary conditions for the applied bias. The piezoelectric polarization charge is reduced due to the electromechanical coupling compared to the uncoupled case. Under high sheet electron densities, the correction in the piezoelectric polarization charge is also lower due to smaller electric field.

A particle based device simulator that couples the Poisson solver and the Monte Carlo Transport kernel has been developed to implement the theoretical model for electromechanical coupling for a GaN/AlGaN/AlN/GaN HEMT device. It has been observed that the coupled formulation leads to degradation in the drain current that varies from 2% to 18%. The degradation in the drain current is the largest near the threshold voltage and reduces for more positive gate voltages. This behavior can be easily explained using the charge argument. Namely for large negative bias, there is almost no inversion charge density in the channel and the vertical fields area high. For zero bias on the gate, the inversion charge is the highest and it balances the net positive spontaneous

and polarization charge density, hence the vertical field is the smallest. The same trend is also observed in the transfer characteristics of the device.

An electro-thermal particle based device simulator consisting of a Monte Carlo-Poisson equation solver that is self consistently coupled with an energy balance solver for both the acoustic and optical phonon baths has been developed to understand the physics behind the self heating phenomenon in these devices. An output current degradation of around 2-3% at Vds = 5V and Vgs = 0V has been observed in simulations. It is observed that the electrostatics in the device is modified with the inclusion of the self heating effects. The electric field near the gate-drain edge is modified in a direction to accelerate the electrons from the channel towards the surface states of the device. The trapping de-trapping of these defects can lead to further degradation in the performance of these devices due to self heating effects. This study has also proved that the electrostatics near the gate-drain edge is a very critical for a reliable performance of these devices. Simulations have been done emulating the charging of the surface states due to high D.C. stress. Degradation of output characteristics have been observed and match very well with experimental data.

The effect of shielding these devices on the impact on the reliability issues in these devices has also been investigated. It has been observed that with the shield electrode the electric field in the device can be spread to a wider region, thus reducing the electric field at the gate-drain edge of the device. As the peak electric field moves far away from the gate-drain edge, the peak electron velocity also moves with it. The peak lattice temperature follows the peak electron velocity, as the energy of the electrons is

highest in this region. This reduces the impact of self heating on the performance of these devices.

In this work, buck converter being one of the most important computing segment applications for Power MOSFET has been studied in great detail. Mixed mode simulations utilizing TCAD device models have been performed for a state of the art Silicon Trench Power MOSFET. The various loss mechanisms associated with the FETs, the device parameters that relate to these loss mechanisms and the design considerations to improve the efficiency performance of the device has also been presented in great detail. These simulations have excellent agreement with real application data and the significance of the parasitic present in the circuit has also been addressed. The advantages of GaN FETs over Silicon FETs in these applications and design consideration for further improvement have also been presented.

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